FEATURES

- Drives both high-side and low-side MOSFETs in a synchronous buck configuration
- Large drivers designed to drive 4nF server class FETs
  - Low side driver - 3A source / 6A sink
  - High side driver – 3A source / 4A sink
  - Transitions times & Propagation delays < 20ns
- Fixed 12V gate Drive
- Integrated bootstrap diode
  - Reduces external component count
- Capable of high switching frequencies from 200kHz up to 1MHz
- Configurable PWM modes of operation
  - CHiL Active Tri-Level (ATL), disables both MOSFETs in 30ns with no hold-off time
  - Generic tristate PWM with hold-off
- Adaptive non-overlap protection minimizes diode conduction time
- Input supply under voltage protection
- Thermally enhanced 10 pin DFN package
- Lead free RoHS compliant package, MSL level 1

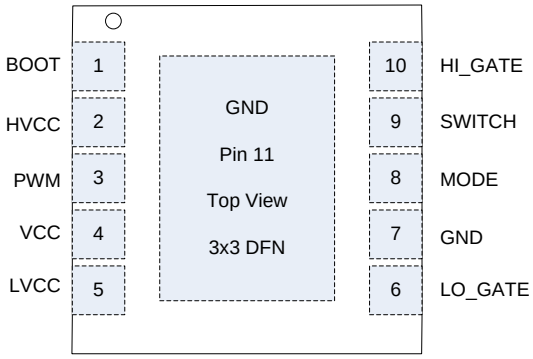

Figure 1. CHL8511 10 pin DFN Package

DESCRIPTION

The CHL8511 MOSFET is a high efficiency gate driver which can switch both high-side and low-side N-channel external MOSFETs in a synchronous buck converter. It is intended for use with CHiL Digital PWM controllers to provide a total voltage regulator (VR) solution for today's advanced computing applications.

The CHL8511 low side driver is capable of rapidly switching large MOSFETs with low R_{dson} and large input capacitance used in high efficiency designs.

The CHL8511 can be configured to drive both the high and low side switches from the unique CHiL fast Active Tri-Level (ATL) PWM signal or a generic tri-state PWM mode. The CHiL ATL mode allows the controller to disable the high and low side FETS in less than 30ns without the need for a dedicated disable pin. This improves VR transient performance, especially during load release.

The integrated boot diode reduces external component count. The CHL8511 also features an adaptive non-overlap control for shoot-through protection. This prevents cross conduction of both high-side and low-side MOSFETs and minimizes body diode conduction time to provide best in class efficiency.

The CHL8511 is pin compatible with the CHL8510 MOSFET driver.

APPLICATIONS

- Multiphase synchronous buck converter for Server and desktop computers using Intel® and AMD® VR solutions
- High efficiency and compact VRM
- High current DC/DC Converters

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FUNCTIONAL BLOCK DIAGRAM

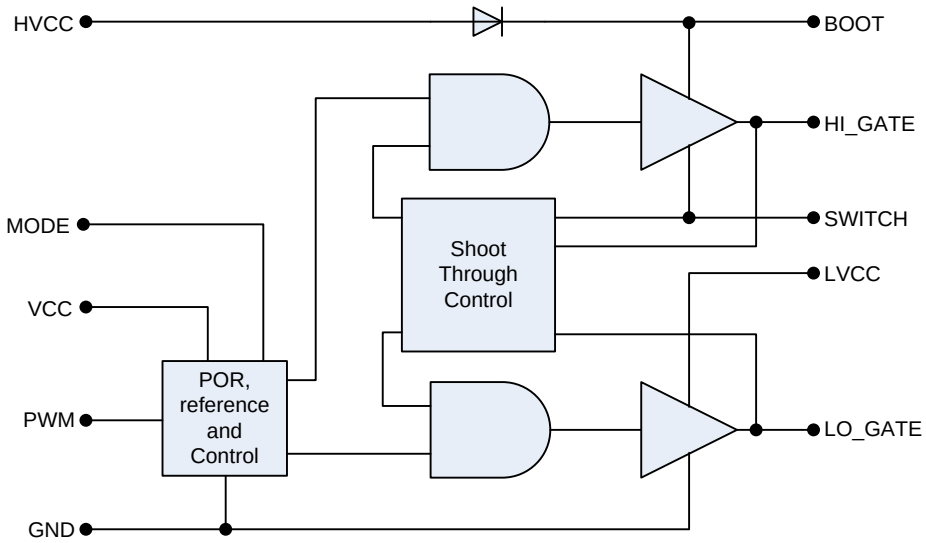


Figure 2. Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	FUNCTION
1	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the SWITCH pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
2	HVCC	Connect this pin to +12V to provide a gate drive voltage on the high-side MOSFETS. This is the anode of the internal bootstrap diode. Place a high quality low ESR ceramic capacitor from this pin to GND.
3	PWM	The PWM signal is the control input for the driver from a 1.8V or 3.3V PWM signal. The PWM signal can enter three distinct states during operation; see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
4	VCC	Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
5	LVCC	Connect this pin to +12V to provide a gate drive voltage on the low-side MOSFETs. Place a high quality low ESR ceramic capacitor from this pin to GND.
6	LO_GATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
7	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
8	MODE	This pin allows selection of the PWM signal voltage for 1.8V or 3.3V normal operation. Floating this pin configures the driver for CHiL Active Tri-Level (ATL) at 1.8V PWM and connecting this pin to ground configures the driver for generic active tri-state operation using 3.3V PWM.
9	SWITCH	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
10	HI_GATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
PAD(11)	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.

TYPICAL APPLICATION

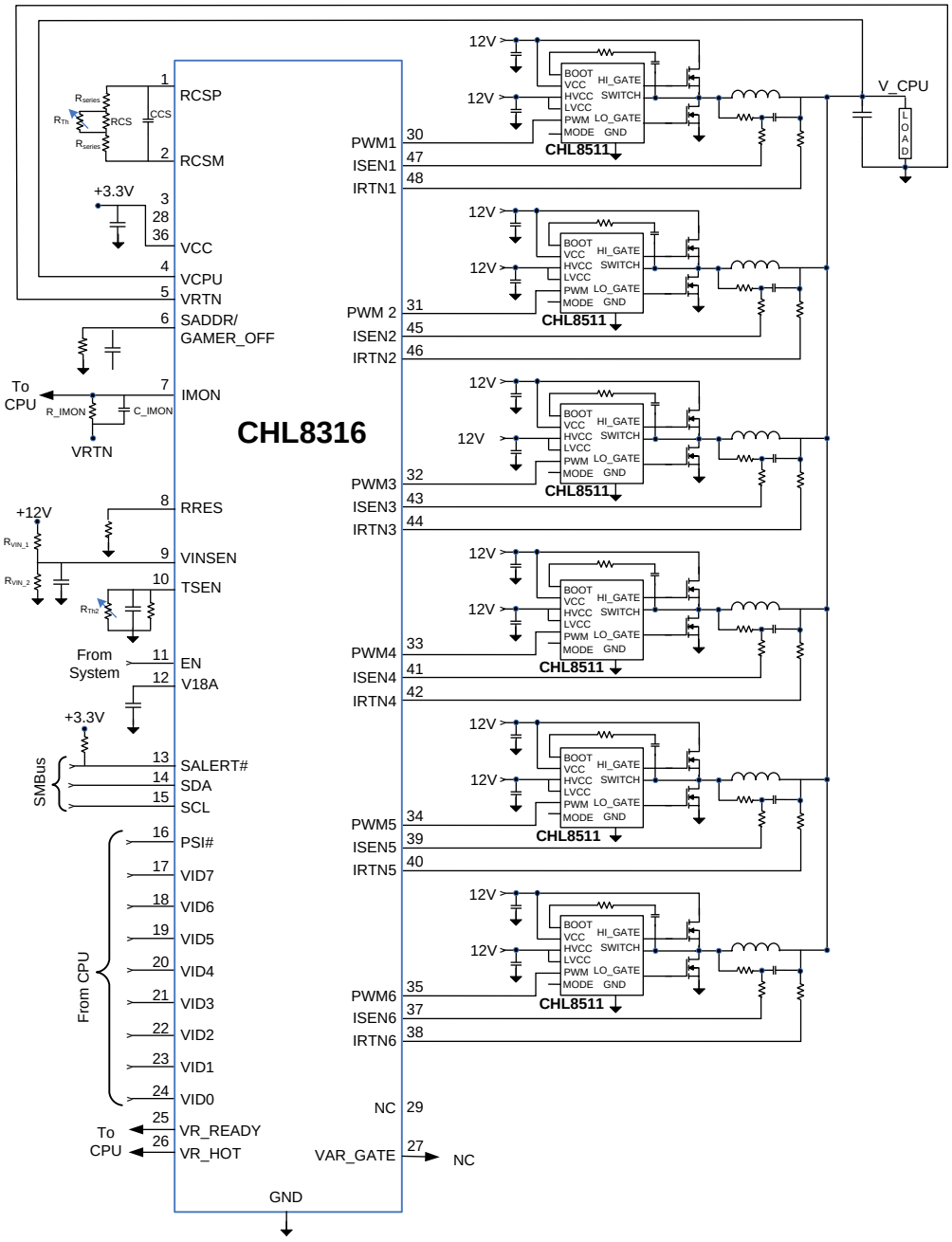


Figure 3. 6-Phase VRD using CHL8511 MOSFET drivers & CHL8316 Controller

ABSOLUTE MAXIMUM RATINGS

BOOT	+35.0V reference to GND +15V reference to SWITCH
PWM	+7.0V
VCC, LVCC, HVCC	+15.0V
LO_GATE	DC : -0.3V to <0.3V above Vcc <200ns: -2V to <0.3V above Vcc
GND	0V+/- 0V
SWITCH	DC: -0.3V to +15V, <20nS: 25V <5nS, -10V, <20 ns: -4Vdc and < 200 ns: -2Vdc
HI_GATE	DC : SWITCH – 0.3V to 0.3V above VBOOT <200ns: SWITCH – 2V to 0.3V above VBOOT
MODE	-0.3V to +15.0V

Recommended Operating Conditions

Operating Ambient Temperature Range	0°C to 85°C
Maximum Operating Junction Temperature	125°C
Supply voltage range (VCC, LVCC, HVCC)	+12V ± 10%

Thermal Information

Thermal Resistance (θ_{JC})	3°C/W
Thermal Resistance (θ_{JA}) (1)	45°C/W
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

NOTES:
1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL SPECIFICATIONS *Recommended Operating Conditions. Tested at +25°C, unless otherwise specified.*

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Bias Current	I_{VCC}	f_{PWM}= 300kHz, V_{VCC}= 12V, no load		7.0		mA
Quiescent Bias Current	I_{DD}			5.0		mA
VCC Rising Threshold for POR				8.6		V
VCC Falling Threshold for POR				7.1		V
PWM INPUT CHiL ATL mode (See Figure 4)						
PWM Input High Threshold	$V_{IH(C\_PWM)}$	VCC = 12V		1.0		V
PWM Input Low Threshold	$V_{IL(C\_PWM)}$	VCC = 12V		0.8		V
PWM Tri-level Hi threshold	$V_{TL(C\_PWM)}$	VCC = 12V		2.65		V
PWM Tri-level Low threshold	$V_{TH(C\_PWM)}$	VCC = 12V		2.55		V
PWM Input Current Low	I_{C_PWM}	V_{pwm}= 0V		-0.88		mA
PWM Input Current Hi		V_{pwm}= 3.3V		-10		µA
PWM INPUT Tristate Mode (See Figure 5)						
PWM Input rising Threshold	$V_{IH(C\_PWM)}$	VCC = 12V		1.65		V
PWM Input falling Threshold	$V_{IL(C\_PWM)}$	VCC = 12V		1.3		V
Tri-State LO_GATE Threshold				0.85		V
Tri-State LO_GATE Hysteresis				200		mV
Tri-State HI_GATE Threshold				2.55		V
Tri-State HI_GATE Hysteresis				200		mV

ELECTRICAL SPECIFICATIONS (contd.)

Tri-State hold off time				80		ns
PWM Input Pull-up voltage	V_{PWM_pullup}	PWM input floating		1.65		V
PWM Input Resistance	R_{PWM}	PWM input floating		3.75		kΩ
HIGH SIDE GATE DRIVER						
Transition Time – Rise	$t_{R(HS)}$	6nF Load, V_{VCC}= 12V, 10% - 90%	-	21	-	ns
Transition Time - Fall	$t_{F(HS)}$	6nF Load, V_{VCC}= 12V, 10% - 90%	-	18	-	ns
Transition Time – Rise	$t_{R(HS)}$	3nF Load, V_{VCC}= 12V, 10% - 90%	-	15	-	ns
Transition Time - Fall	$t_{F(HS)}$	3nF Load, V_{VCC}= 12V, 10% - 90%	-	12	-	ns
Propagation Delay - Turn-On	$t_{PDH(HS)}$	6nF Load, V_{VCC}= 12V, Adaptive	-	16	-	ns
Propagation Delay - Turn-Off	$t_{PDL(LS)}$	6nF Load, V_{VCC}= 12V	-	17	-	ns
Propagation Delay – Exit Tristate	$t_{PDTS(HS\_en)}$	6nF Load, V_{VCC}= 12V		29		ns
Propagation Delay- Enter Tristate	$t_{PDTS(HS\_dis)}$	6nF Load, V_{VCC}= 12V		16		ns
Source Current	I_{HS_SOURCE}	6nF Load, V_{VCC}= 12V	-	3.0	-	A
Output Impedance source	R_{HS_SOURCE}	Sink Current at 100mA		1.6		Ω
Sink Current	I_{HS_SINK}	6nF Load, V_{VCC}= 12V	-	4.0	-	A
Output impedance - Sinking	R_{HS_SINK}	Sink Current at 100mA		0.6	.	Ω
LOW SIDE GATE DRIVER						
Transition Time - Rise	$t_{F(LS)}$	6nF Load, V_{VCC}= 12V, 10% - 90%	-	18	-	ns
Transition Time - Fall	$t_{R(LS)}$	6nF Load, V_{VCC}= 12V, 10% - 90%	-	13	-	ns
Transition Time - Rise	$t_{F(LS)}$	3nF Load, V_{VCC}= 12V, 10% - 90%	-	13	-	ns
Transition Time - Fall	$t_{R(LS)}$	3nF Load, V_{VCC}= 12V, 10% - 90%	-	9	-	ns
Propagation Delay - Turn-On	$t_{PDH(LS)}$	6nF Load, V_{VCC}= 12V, Adaptive	-	17	-	ns
Propagation Delay - Turn-Off	$t_{PDL(LS)}$	6nF Load, V_{VCC}= 12V	-	13	-	ns
Propagation Delay – Exit Tristate	$t_{PDTS(LS\_en)}$	6nF Load, V_{VCC}= 12V		26		ns
Propagation Delay - Enter Tristate	$t_{PDTS(LS\_dis)}$	6nF Load, V_{VCC}= 12V		14		ns
Source Current	I_{LS_SOURCE}	6nF Load, V_{VCC}= 12V	-	4.0	-	A
Output impedance - Sourcing	R_{LS_SOURCE}	Sink Current at 100mA		1.5		Ω
Sink Current	I_{LS_SINK}	6nF Load, V_{VCC}= 12V	-	6	-	A
Output Impedance - Sinking	R_{LS_SINK}	Sink Current at 100mA		0.4		Ω

TIMING DIAGRAMS

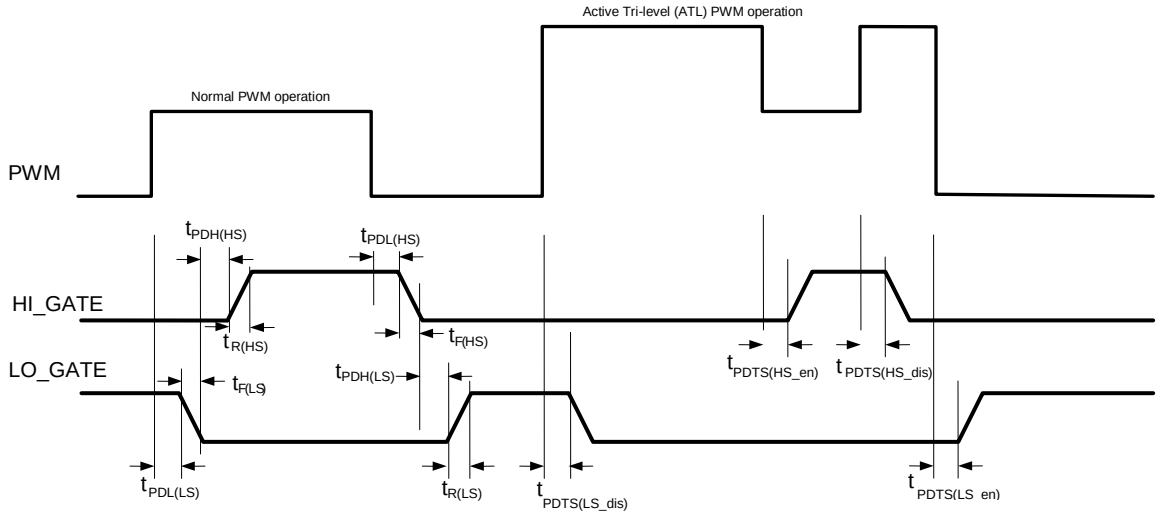


Figure 4. CHiL Active Tri-Level (ATL) mode PWM, HI_GATE and LO_GATE signals

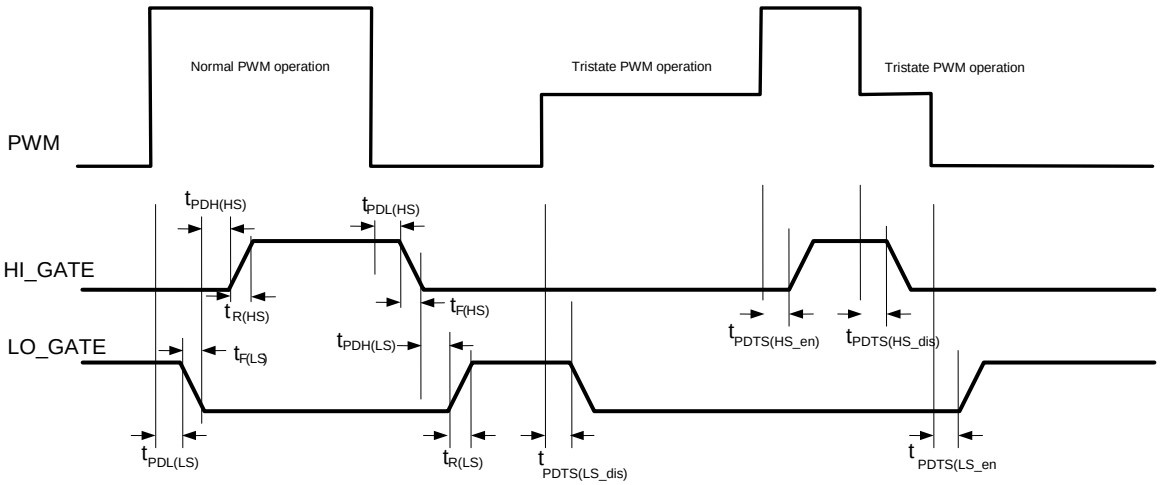


Figure 5. Tristate mode PWM, HI_GATE and LO_GATE signals

GENERAL DESCRIPTION

The CHL8511 is a high efficiency, fast MOSFET driver with large source and sink current capability. It can reliably drive the external high- and low-side N-channel MOSFETs with large input capacitance at switching frequencies up to 1MHz. The proprietary CHiL Active Tri-Level (ATL) feature allows complete control over enable and disable of both MOSFETs using the PWM input signal from the controller. The driver is also compatible with a generic tri-state PWM signal. ATL or tri-state is selectable by the MODE pin.

During normal operation the PWM transitions between low and high voltage levels to drive the low- and high-side MOSFETs. The PWM signal falling edge transition to a low voltage threshold initiates the high side driver turn off after a short propagation delay, $t_{PDL(HS)}$. The dead time control circuit monitors the HI_GATE and switch voltages to ensure the high side MOSFET is turned off before the LO_GATE voltage is allowed to rise to turn on the low-side MOSFET.

The PWM rising edge transition through the high-side turn on threshold, initiates the turn off of the low-side MOSFET after a small propagation delay, $t_{PDL(LS)}$. The adaptive dead time circuit provides the appropriate dead time by determining if the falling LO_GATE voltage threshold has been crossed before allowing the HI_GATE voltage to rise and turn on the high-side MOSFET, $t_{PDH(HS)}$.

THEORY OF OPERATION

Power-on Reset (POR)

The CHL8511 incorporates a power-on reset feature. This ensures that both the high and low side output drivers are made active only after the device supply voltage has exceeded a certain minimum operating threshold. The V_{cc} supply is monitored and both the drivers are set to the low state, holding both external MOSFETs off. Once V_{cc} crosses the rising POR threshold, the CHL8511 is reset and the outputs are held in the low state until a transition from tri-state to active operation is detected at the PWM input. During normal operation the drivers continue to remain active until the V_{cc} falls below the falling POR threshold.

These POR voltage threshold levels allow seamless functionality with the CHiL digital controllers, such that the drivers are always active before the controller starts to provide the PWM signal and are inactive only after the controller shuts down.

Integrated Bootstrap Diode

The CHL8511 features an integrated bootstrap diode to reduce external component count. This enables the CHL8511 to be used effectively in cost and space sensitive designs.

The bootstrap circuit is used to establish the gate voltage for the high-side driver. It consists of a diode and capacitor connected between the SWITCH and BOOT pins of the device. Integrating the diode within the CHL8511, results in the need for an external boot capacitor only. The bootstrap capacitor is charged through the diode and injects this charge into the high-side MOSFET input capacitance when PWM signal goes high.

PWM Mode Selection

The CHL8511 features a MODE pin which allows operation with different PWM signal levels. The CHL8511 is capable of driving external MOSFETs based on one of two different tri-level PWM input signals from a controller.

Floating the MODE pin enables the CHL8511 to switch external FETs based on the CHiL proprietary ATL mode. In ATL mode, the PWM voltage level is from 0V to 1.8V for low to high transitions. A PWM voltage level greater than the tristate HI_GATE threshold disables switching of both MOSFETs. Grounding the MODE pin enables the CHL8511 to switch FETs based on a generic tri-state signaling with the PWM signal from 0V to 3.3V for low to high transitions. A PWM voltage level in the tri-state window of 1.23VDC and 1.82VDC for 80ns results in disabling both external MOSFETs.

CHiL Active Tri-Level (ATL) PWM input signal

The CHL8511 gate drivers are driven by a unique tri-level PWM control signal provided by the CHiL digital PWM controllers. During normal operation, the rising and falling edges of the PWM signal transitions between 0V and 1.8V to switch the LO_GATE and HI_GATE. To force both driver outputs low simultaneously, the PWM signal crosses a tri-state voltage level higher than the tristate HI_GATE threshold. This threshold based tri-state results in a very fast disable with only a small tri-state propagation delay. MOSFET switching resumes when the PWM signal falls below the tri-state threshold into the normal operating voltage range.

This fast tri-state operation eliminates the need for the PWM signal to dwell in the shutdown window, eliminating any hold-off time. In addition, the disable delay time is not affected by the PWM trace routing capacitance. A Dedicated enable pins is not required which simplifies the

routing and layout in applications with a limited number of board layers. It also provides switching free of shoot through for PWM transition times of up to 20ns. The CHL8511 is therefore tolerant of stray capacitance on the PWM signal lines.

The CHL8511 provides a 0.88mA typical pull-up current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. The 0.88mA typical current is designed for driving worst case stray capacitances and transition the CHL8511 into the tri-state condition rapidly to avoid a prolonged period of conduction of the high or low side MOSFETs during faults. Once the PWM signal has been pulled up, the current is disabled to reduce power consumption.

Diode Emulation during load release

One advantage of ATL is the ability to quickly turn-off all low side MOSFETs during a load release event. This is known as diode emulation since all the load current is forced to flow momentarily through the body diodes of the MOSFETs. This results in a much lower overshoot on the output voltage as can be seen in Figure 6 below.

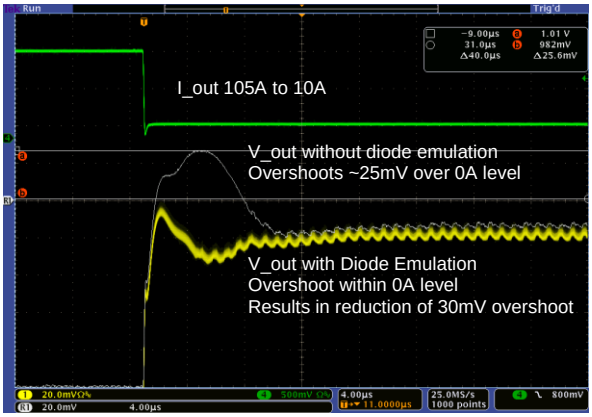


Figure 6. Output voltage overshoot reduction with diode emulation

Start Up

During initial startup, the CHL8511 holds both high- and low-side drivers low even after POR threshold is reached. This mode is maintained while the PWM signal is pulled to the tri-state threshold level greater than the tri-state HI_GATE threshold and until it transitions out of tri-state. It is this initial transition out of the tri-state which enables both drivers to switch based on the normal PWM voltage levels.

This startup also ensures that any undetermined PWM signal levels from a controller in pre-POR state will not result in high or low side MOSFET turn on until the controller is out of its POR.

High Side Driver

The high-side driver drives an external floating N-channel MOSFET which can be switched at up to 1MHz. An external bootstrap circuit referenced to the SWITCH node, consisting of a boot diode and capacitor is used to bias the external MOSFET gate. When the SWITCH node is at ground, the boot capacitor is charged to the voltage on the HVCC pin less the forward drop of the diode. This stored charge is used to turn on the high-side MOSFET when the PWM signal goes high. Once the high-side MOSFET is turned on, the SWITCH voltage raises to the supply voltage and the boot voltage to equal to the supply voltage plus the HVCC voltage less the diode forward voltage.

When the PWM signal goes low, the MOSFET is turned off by pulling the MOSFET gate to the SWITCH voltage.

Low Side Driver

The CHL8511 low-side driver is designed to drive an external N-channel MOSFET referenced to ground at up to 1MHz. The low-side driver is connected internally to the LVCC supply voltage..

Adaptive dead time adjustment

In a synchronous buck configuration, dead time between the turn off of one gate and turn on of the other is necessary to prevent simultaneous conduction of the external MOSFETS preventing a shoot-through condition which would result in a short of the supply voltage to ground. A fixed dead time does not provide optimal performance across a variety of MOSFETsand board layouts.

The CHL8511 provides an ‘adaptive’ dead time adjustment. This feature minimizes dead time which maximizes efficiency. The ‘break before make’ adaptive design is achieved by monitoring gate and SWITCH voltages to determine OFF status of a MOSFET. It also provides zero-voltage switching (ZVS) of the low side MOSFET with minimum current conduction through its body-diode.

When the PWM is switching between 1.8V and 0V, its falling edge transition from high to low will turn off the high side gate driver. The adaptive dead time circuit monitors the HI_GATE and the SWITCH node voltages during the high-side MOSFET turn off. When the HI_GATE falls below 1.7V above the SWITCH node potential or the SWITCH node voltage drops below 0.8V, the high-side MOSFET is determined to be turned off and the LO_GATE turn-on is

initiated. This turns on the external low-side MOSFET. The rising edge transition of the PWM signal from low to high voltage causes the low-side gate driver to turn off. The adaptive circuit monitors the voltage at LO_GATE and when it falls below 1.7V, the low-side MOSFET is determined to be turned off and the high-side MOSFET turn-on is initiated. This turns on the external high-side MOSFET.

APPLICATION INFORMATION

Figure 7 shows the typical applications circuit for the CHL8511.

Bootstrap circuit

Once the high-side MOSFET selection is made, the bootstrap circuit can be defined. The integrated boot diode of the CHL8511 reduces the external component count for use in cost and space sensitive designs. For ultra high efficiency designs, an external bootstrap diode is recommended.

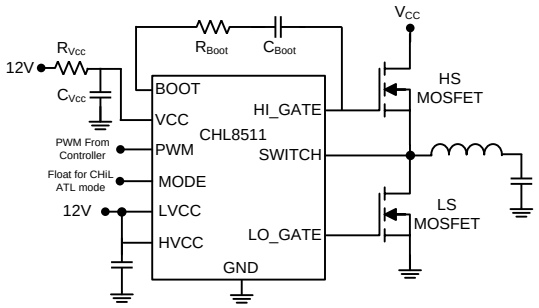


Figure 7. CHL8511 Applications circuit

The bootstrap capacitor C_{Boot} stores the charge and provides the voltage required to drive the external high side MOSFET gate. The minimum capacitor value can be defined by:

$$C_{Boot} = Q_{HS\ MOSFET\_gate} / \Delta V_{Boot}$$

where,

$Q_{HS\ MOSFET\_gate}$ is the total gate charge of the high-side external MOSFET(s)

ΔV_{Boot} is the droop allowed on the boot capacitor voltage (at the high-side MOSFET gate)

If an external boot diode is used, D_{Boot} must capable of handling the average and peak currents, I_{D_avg} and I_{D_peak}, and also the maximum supply voltage.

$$I_{D\_avg} = Q_{HS\ MOSFET\_gate} \times F_{sw\_max}$$

where,

F_{sw_max} is the controller's maximum switching frequency

The I_{D_peak} rating of the diode is determined by actual circuit measurements.

A series resistor (Rboot) of 1Ω to 4Ω, is added to limit the surge current into the boot capacitor on start-up. This resistor can also be used to set the rising slew rate of the high-side MOSFET gate drive (HI_GATE) to help slow the rise time of the switch node for reduced ringing.

Supply decoupling capacitor

Decoupling to the CHL8511 is provided by a bypass capacitor C_{Vcc} located close to the supply input pin. A 1µF, low ESR, multilayer ceramic capacitor is recommended. A series resistor Rvcc, typically 10Ω, is added in series with the supply voltage to filter high frequency ringing and noise.

PCB Layout considerations

PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- High current paths like the gate driver traces should be as wide and short as practically possible.
- Trace inductances to the high and low side MOSFETs should be minimized.
- The ground connection of the IC should be as close as possible to the low side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance.

ORDERING INFORMATION

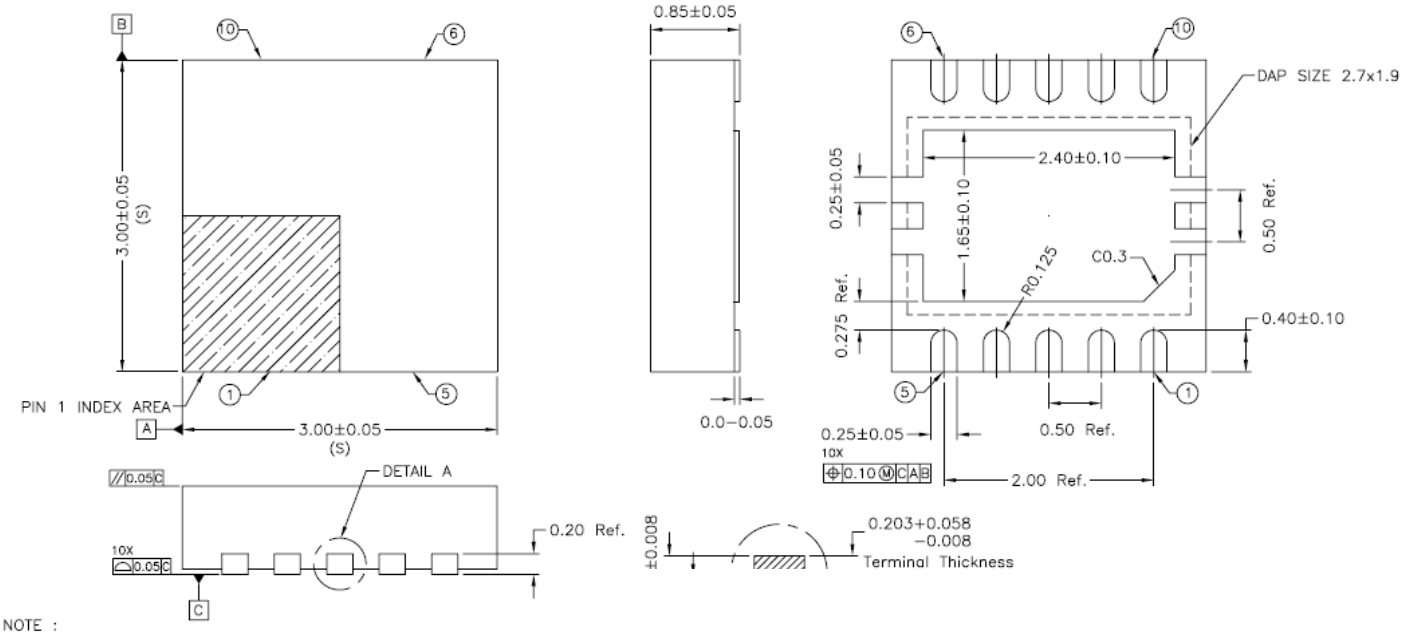
CHL8511 □ □ □

- T: Tape & Reel
- Package type
  R: DFN
- Operating Temperature Range
  C: Commercial Standard

Package	Tape & Reel Qty	Part Number
DFN	3000	CHL8511CRT

PACKAGE INFORMATION

10 pin DFN package



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. REFER JEDEC MO−229.