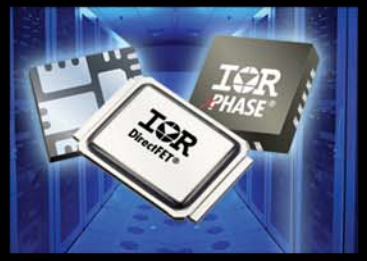
Class D Amplifier Design Basics II

02/19/2009
Rev 1.0



International
IOR Rectifier

Contents

Chapter 1:
Getting Familiar with Class D Audio Amplifier

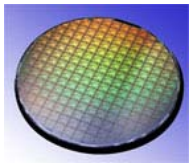
Audio Amplifier Market Trend

A Wire with Gain

- More Channels
- Smaller Box
- Lighter Weight
- More Functions

(Digital Input, Diag)

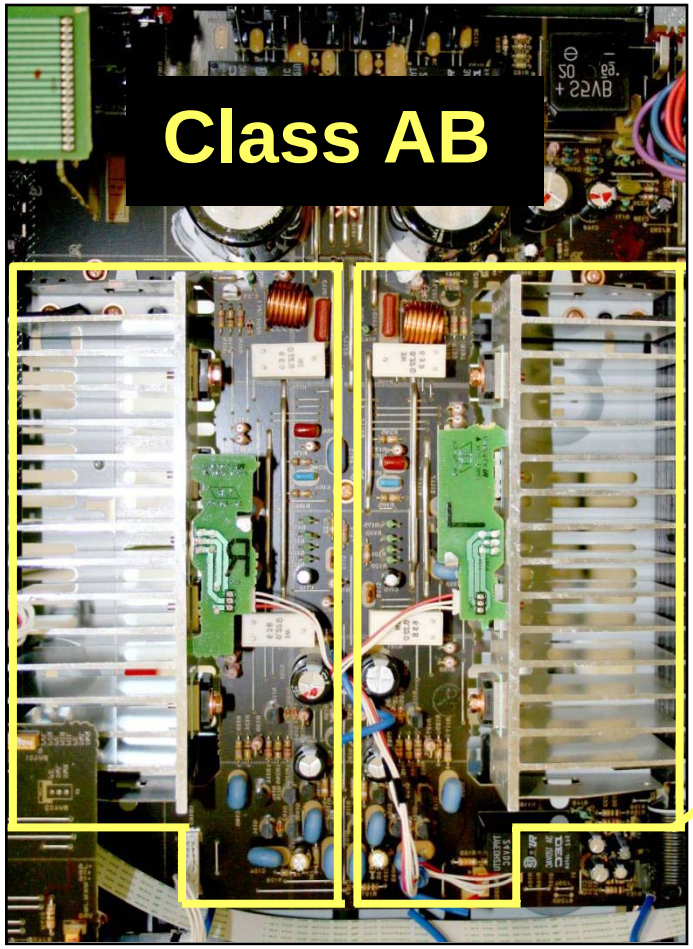
Device Technology



- **Smaller Size**
- **Lower Cost**
- **Audio Performance**

Control Technology

Why Class D Now?



Audio Market Trend

- More Channels
- Smaller Size

- **Smaller Size**

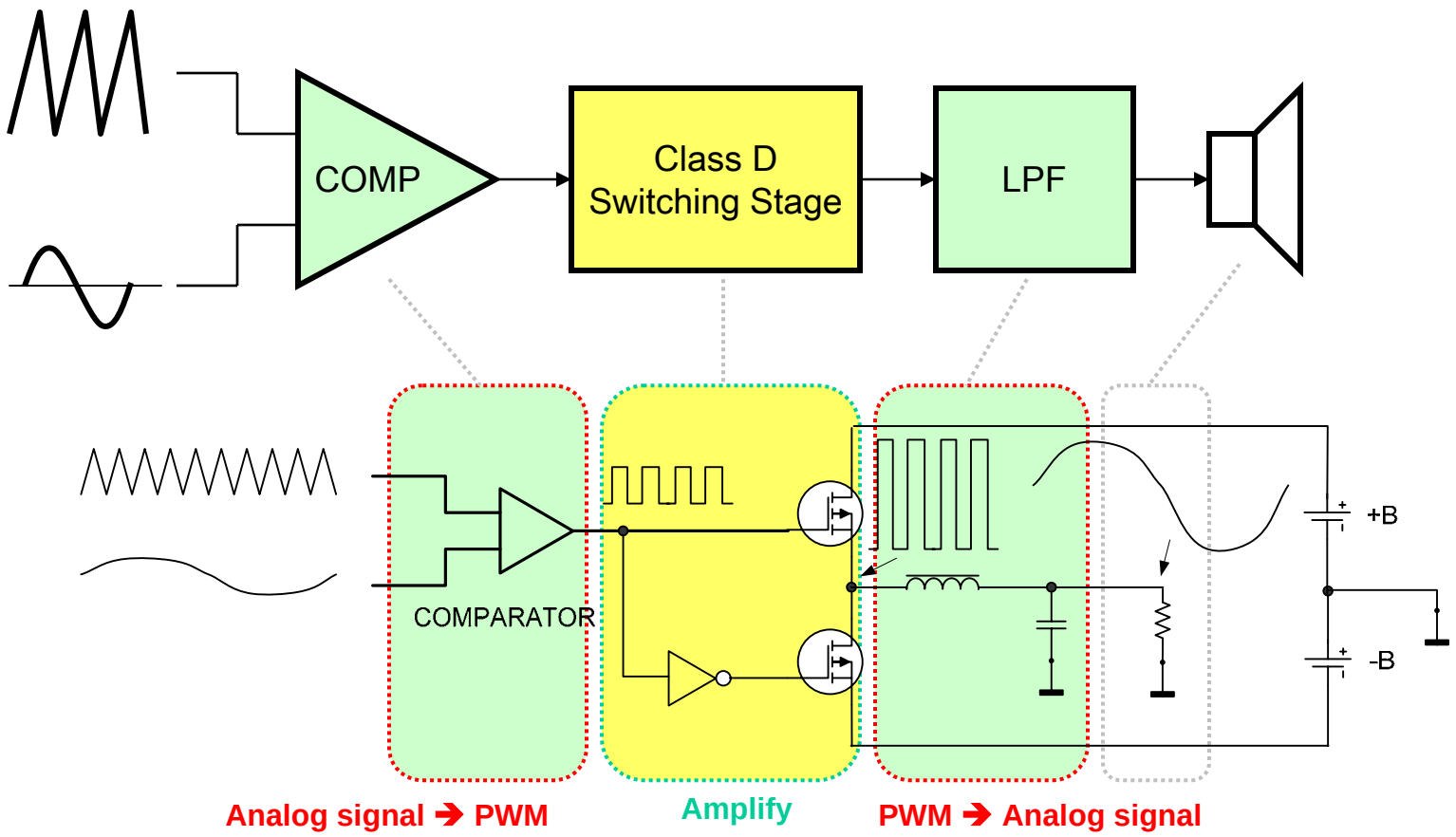
IR Class D

- **Higher Performance**

Device Technology

- MOSFET
- High Speed HVIC

Basic Concept of Class D Audio Amplifier

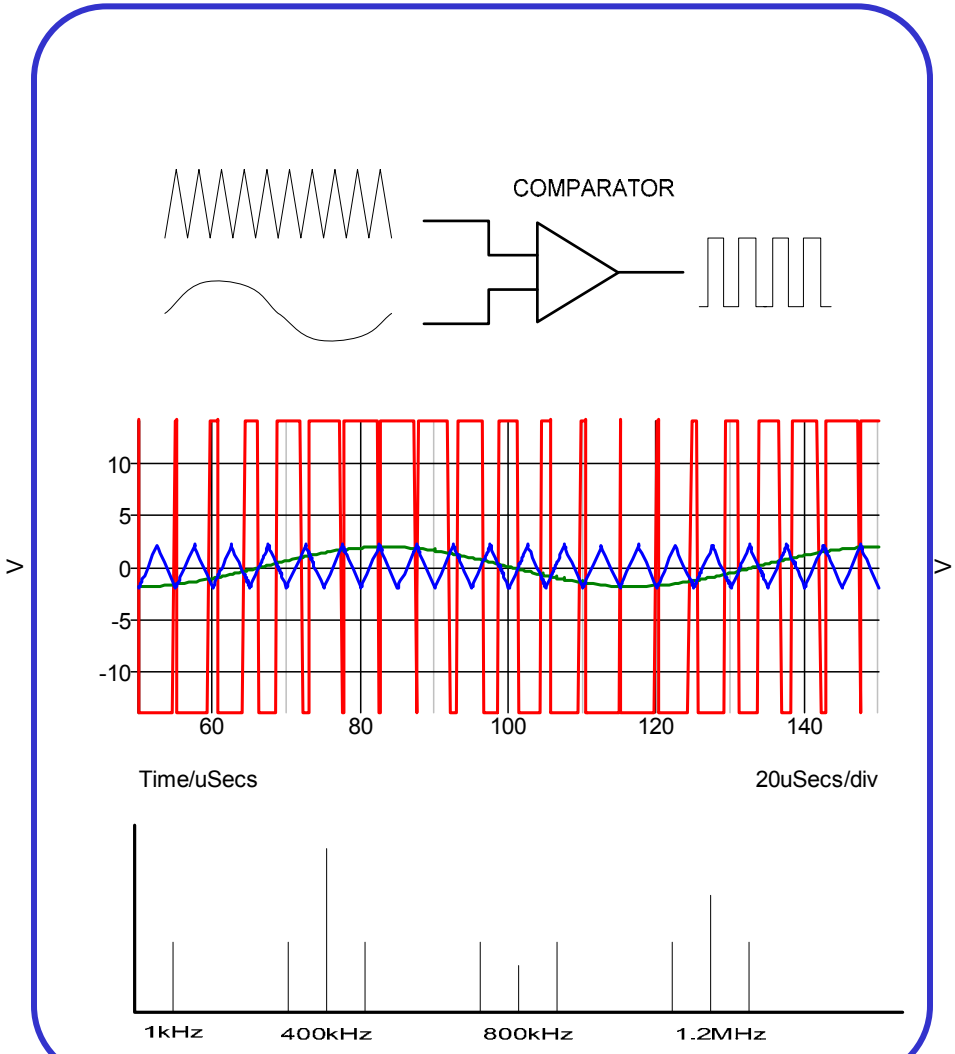


V_{OUT} = B (2D-1)

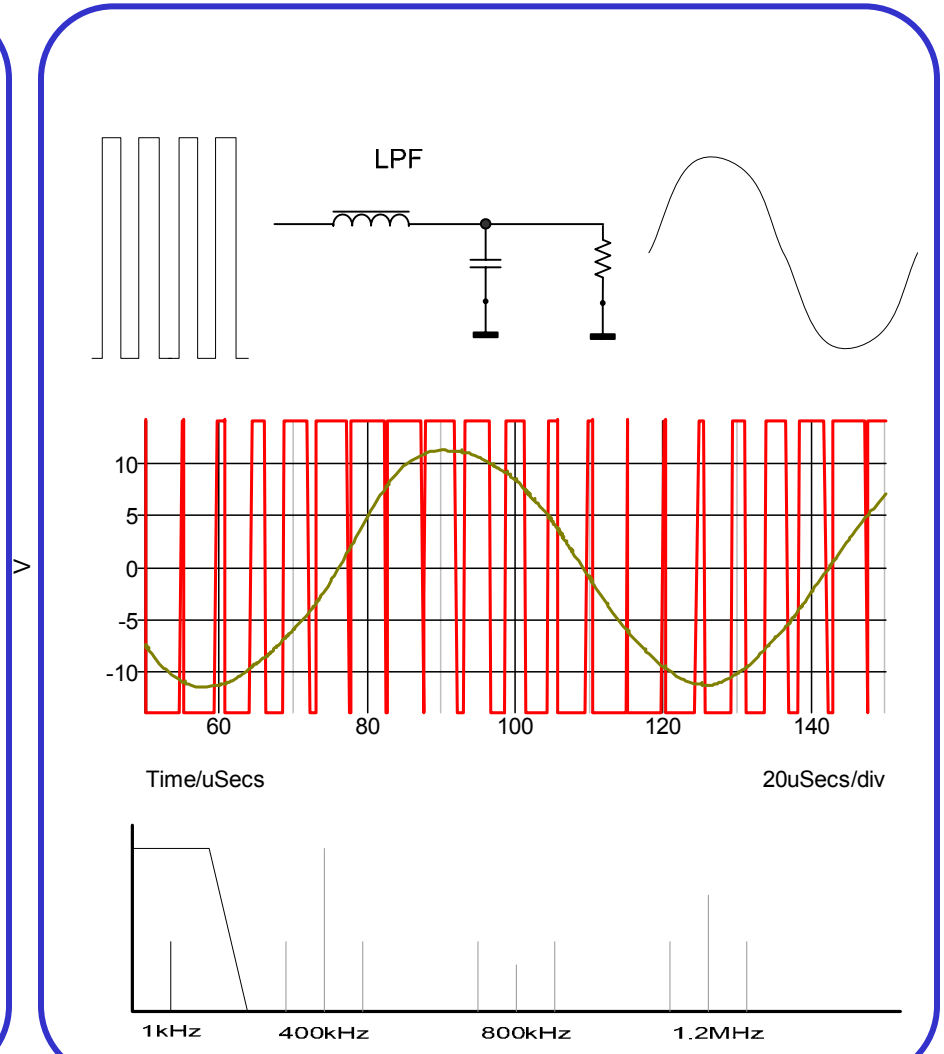
In concept, Class D amplifier is linear; i.e. 0% distortion.

PWM: Heart of Class D Operation

Audio signal ➔ PWM

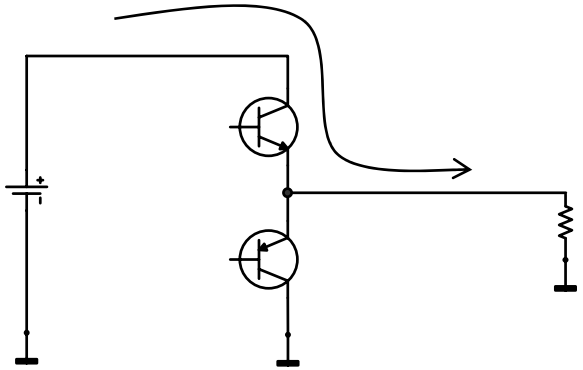


PWM ➔ Audio signal



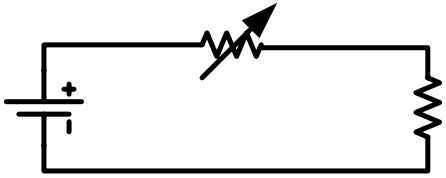
Class AB vs. D Energy Point of View

Class AB



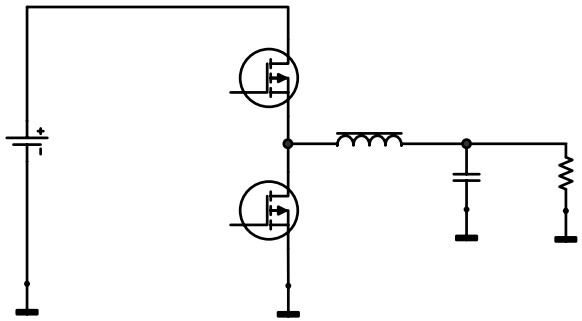
$I_{IN} = I_{OUT}$

Similar to a variable resistor



P_{LOSS} depends on output power factor

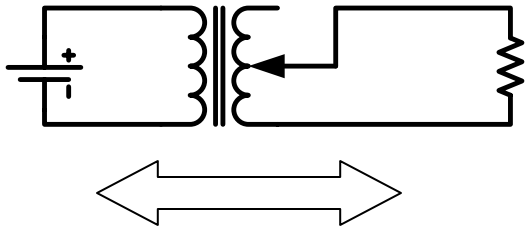
Class D



$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$

Note that input current and output current are not equal.

Similar to a transformer with variable turn ratio



Bi-directional energy flow

Class AB vs. D Characteristic Comparison (1/2)

Feature	Class D Advantage	Class AB
Efficiency	Superior efficiency	
	Efficiency can be improved with device technology	Efficiency is fixed.
	Suitable to drive lower impedance load	Extremely inefficient when driving lower impedance load.
	Can drive reactive load without significant degradation of efficiency	Extremely inefficient when driving reactive load.
	Requires smaller power supply	
Energy flow	Bi-directional energy flow; any energy reflected from the load is recycled to the power supply. Suitable to drive highly reactive load, such as woofer, speaker system with dividing network, piezo speaker, etc.	All the reflected energy from reactive components and back EMF are consumed dissipating heat
Drivability	Inherently has low output impedance (m ohm range)	The output device has high impedance, ~tens of k ohm. With a strong voltage feedback, Class AB can achieve low output impedance.
	Lower impedance loading does not burden power supply. (Power supply current) ≠ (load current).	Power supply current = load current. For a given output power with decreased load impedance, the supply current and heat dissipation in the output device increase.
	Wide power bandwidth; no extra effort to drive high frequency rated power.	Cross conduction limits high frequency power bandwidth.

Class AB vs. D Characteristic Comparison (2/2)

Feature	Class D Advantage	Class AB
Linearity	Topology is inherently linear without feedback	Output device is non-linear; exponential in BJT, quadratic in MOSFET. Strong feedback is necessary to achieve good linearity.
	Cross over distortion is not in zero crossing area	Cross over distortion is at where load current crosses zero, which is most critical point of operation.
Stability	Thermally stable; gain of the Class D stage, bandwidth, loop-gain are independent of output device temperature.	Output devices in linear operating mode has strong temperature coefficient in gain. Loop-gain is changing dynamically with output power.
	No bias-current thermal compensation	
Noise immunity	Inherently immune to incoming noise; low drive impedance, inductor between the load and amplifier.	Because of strong non-linearity in device and 'exposed' feedback node, weak to RF noise.
Reliability	Higher reliability from less heat. Less metal fatigue in solder joints.	

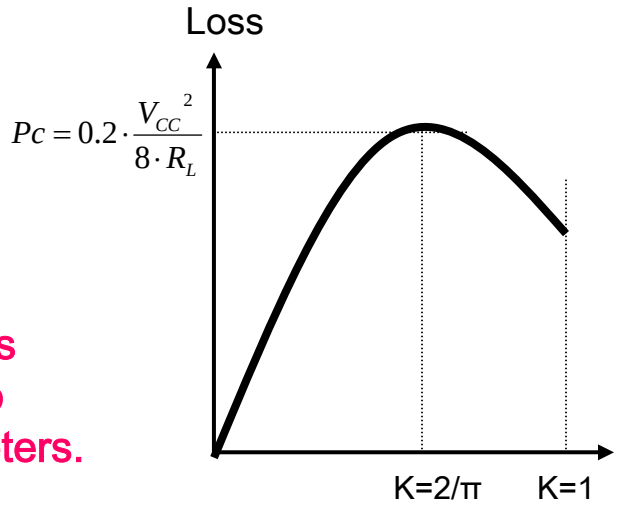
Class AB vs D Comparison

Loss in Class AB

$$P_C = \frac{1}{2\cdot\pi}\cdot\int_0^{\pi}\frac{Vcc}{2}\left(1-K\sin\omega\cdot t\right)\frac{Vcc}{2\cdot R_L}K\sin\omega\cdot t\bullet d\omega\cdot t$$

$$= \frac{Vcc^2}{8\pi\cdot R_L}\cdot\left(\frac{2K}{\pi}-\frac{K^2}{2}\right)$$

Note that this is independent to device parameters.

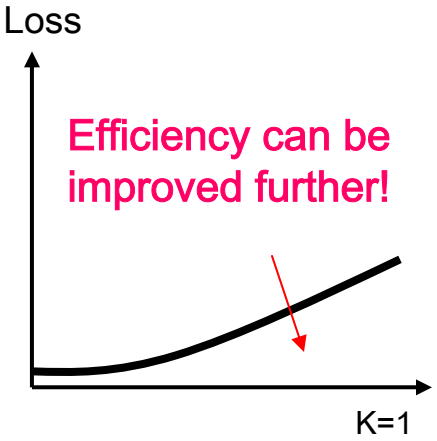


Loss in Class D

$$P_{TOTAL} = Psw + Pcond + Pgd$$

$$Pcond = \frac{R_{DS(ON)}}{R_L}\cdot Po \qquad Pgd = 2\cdot Qg\cdot Vgs\cdot f_{PWM}$$

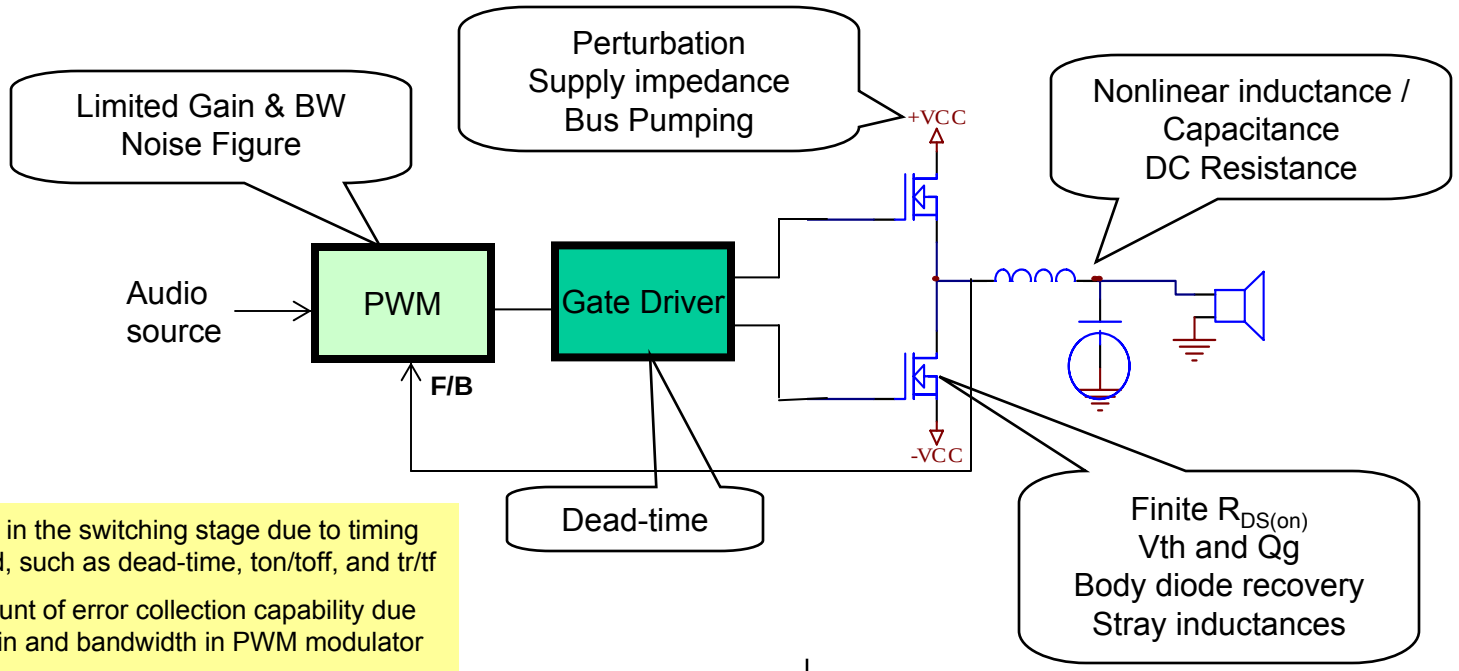
$$Psw = C_{OSS}\cdot V_{BUS}^2\cdot f_{PWM}$$



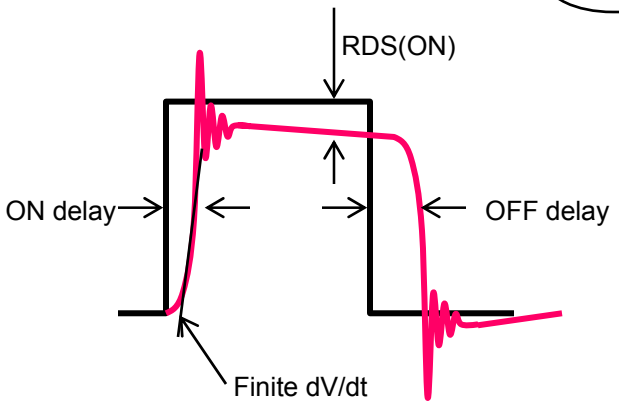
K is a ratio of Vbus and output voltage.

To learn more about power losses in Class D, refer to AN-1070 Class D Amplifier Performance Relationship to MOSFET Parameters.

Practical Class D Amplifier



1. Non-linearity in the switching stage due to timing errors added, such as dead-time, ton/toff, and tr/tf
2. Limited amount of error collection capability due to limited gain and bandwidth in PWM modulator
3. Audio frequency band noise added in PWM modulator
4. Unwanted characteristics in the switching devices, such as finite ON resistance, finite switching speed or body diode characteristics.
5. Parasitic components that cause ringing on transient edges
6. Power supply voltage fluctuations due to its finite output impedance and reactive power flowing through the DC bus
7. Non-linearity in the output LPF.



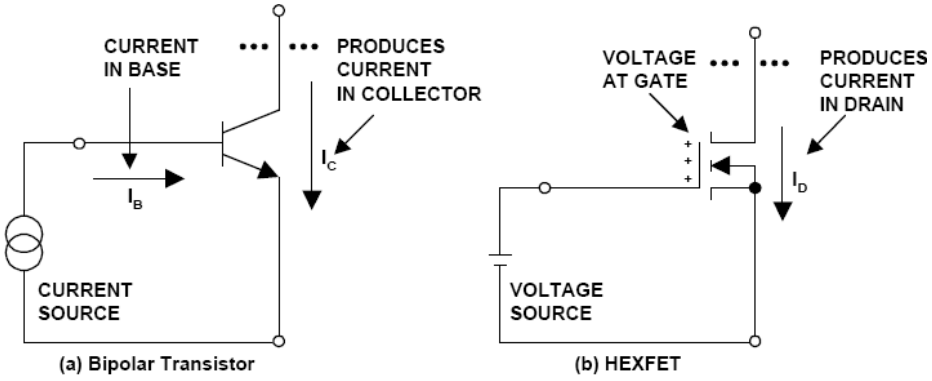
Note that 0.01% of non-linearity corresponds to10mV out of 100V DC bus, or 0.25ns in 400kHz!

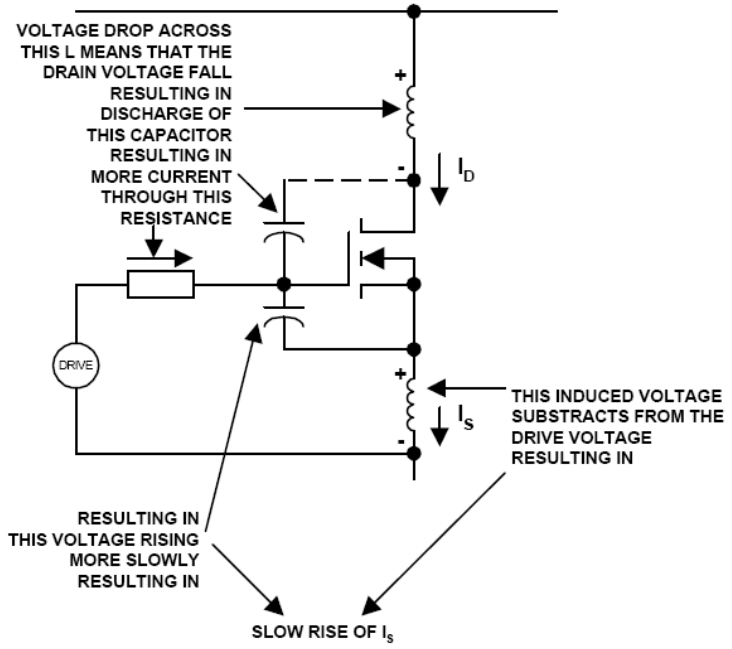
MOSFET Basics

A MOSFET is a device to switch electronic current. A driving MOSFET charges/discharges a capacitor (Gate to Source, Gate to Drain).

A MOSFET does not require any energy to keep it on-state.

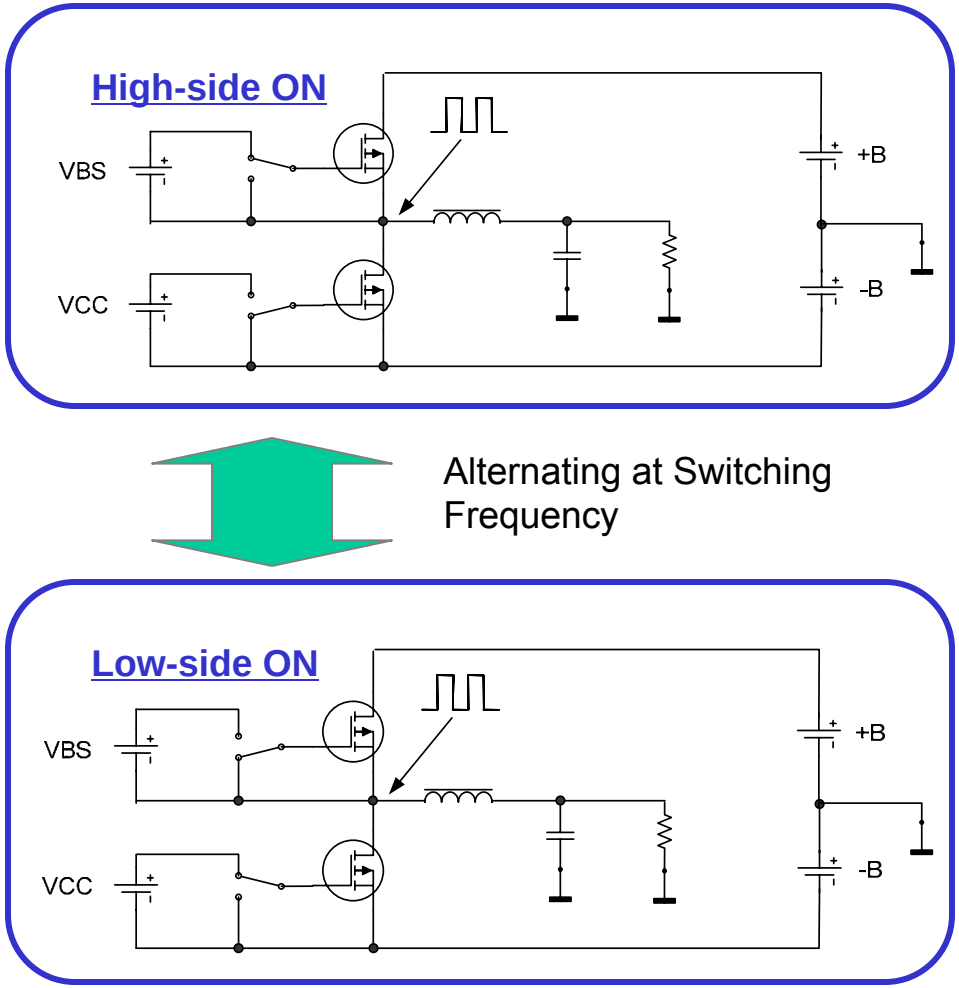
In switching transition, stray impedance in each terminal slows down switching and generates unwanted rings.





To learn more about power MOSFETs, refer to AN-1084 Power MOSFET Basics.

Driving MOSFET for PWM



- Only one side, either high-side or low-side, MOSFET is ON at a time.
- The ratio of ON time between the high-side and low-side MOSFETs determines the output voltage.

Driving a high-side MOSFET

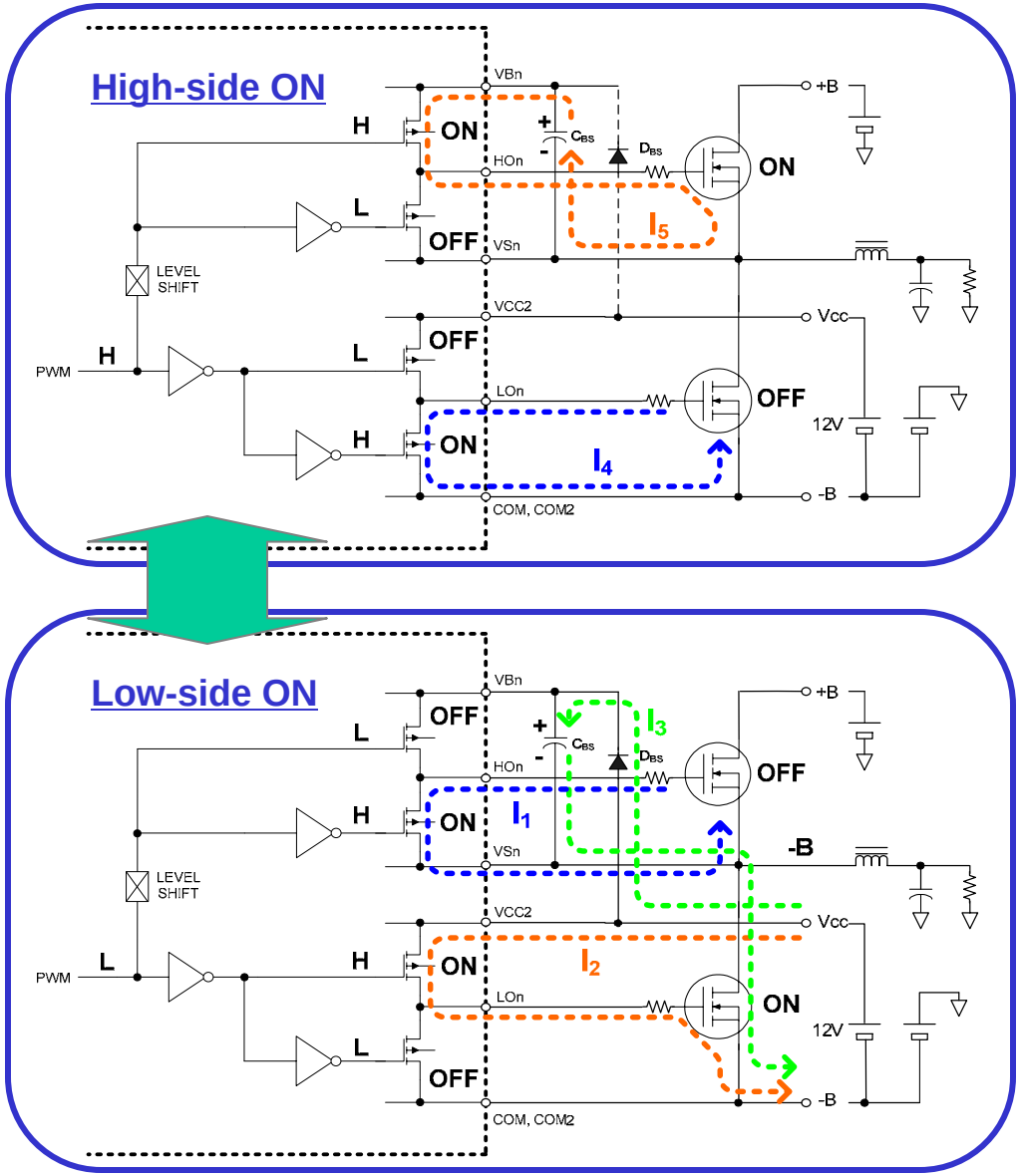
- A floating power supply that referenced to switching node drives the gate of the high-side MOSFET
- The floating power supply is charged when the low-side MOSFET is ON. (Bootstrap power supply)

Driving a low-side MOSFET

- A bias voltage that refers to negative bus voltage –B drives the gate of the low-side MOSFET.

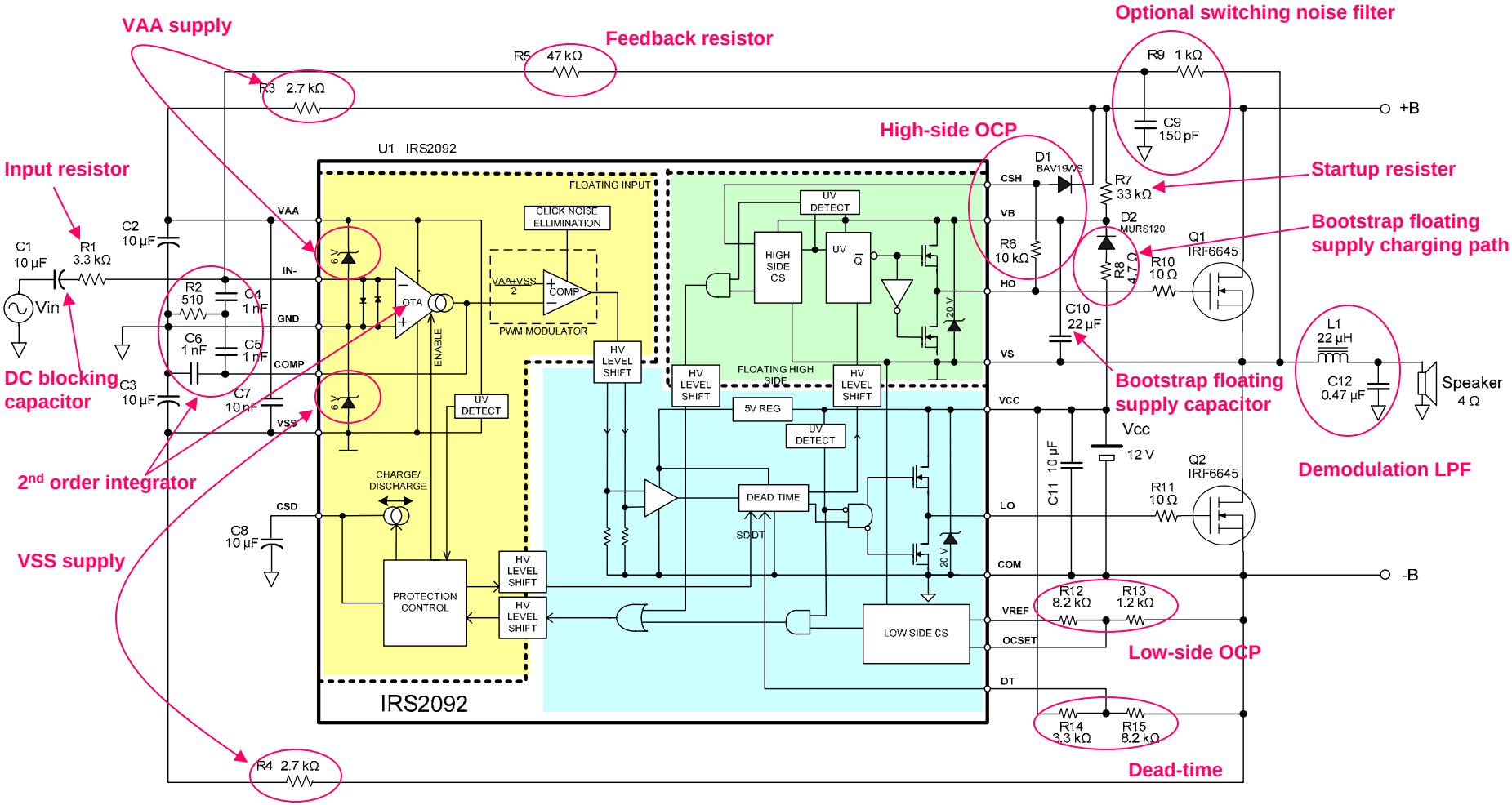
NOTE: In a practical design, a dead-time where both high- and low-side MOSFETs are off is inserted to prevent simultaneous ON state. Refer to chapter 4 for more details.

Bootstrap High Side Power Supply



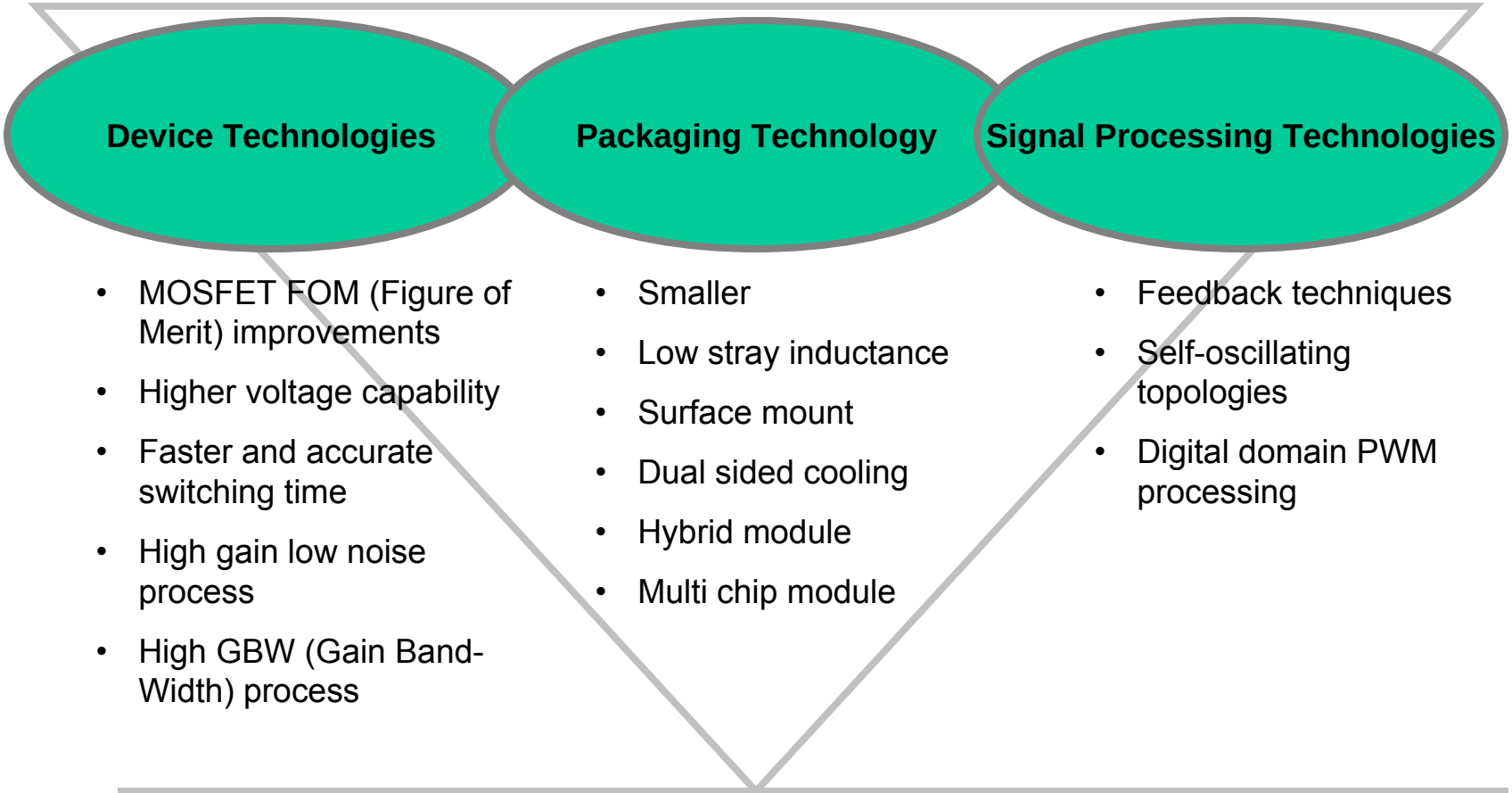
- I_4 turns off the low-side MOSFET. Then, I_5 turns on the high-side MOSFET, lifting VS up to +B. As long as the high side is ON, bootstrap diode D_{BS} isolates the floating power supply VBS and bootstrap capacitor C_{BS} retains V_{BS} voltage.
- After the high-side MOSFET ON state, I_1 turns off the high-side MOSFET, then I_2 turns on the low side MOSFET. As soon as switching node VS reaches negative supply –B, the bootstrap diode D_{BS} turns on and starts charging bootstrap capacitor C_{BS} with current I_3 from V_{CC}.
- Note that $V_{BS} = V_{CC}$ – (forward drop voltage of D_{BS}).

Example of a 100W Class D Amplifier



Chapter 2:
Latest Class D Audio Amplifier Technology Trend

Class D Amplifier Innovations



Higher Performance + Smaller Size + Lower Cost

At The Same Time !

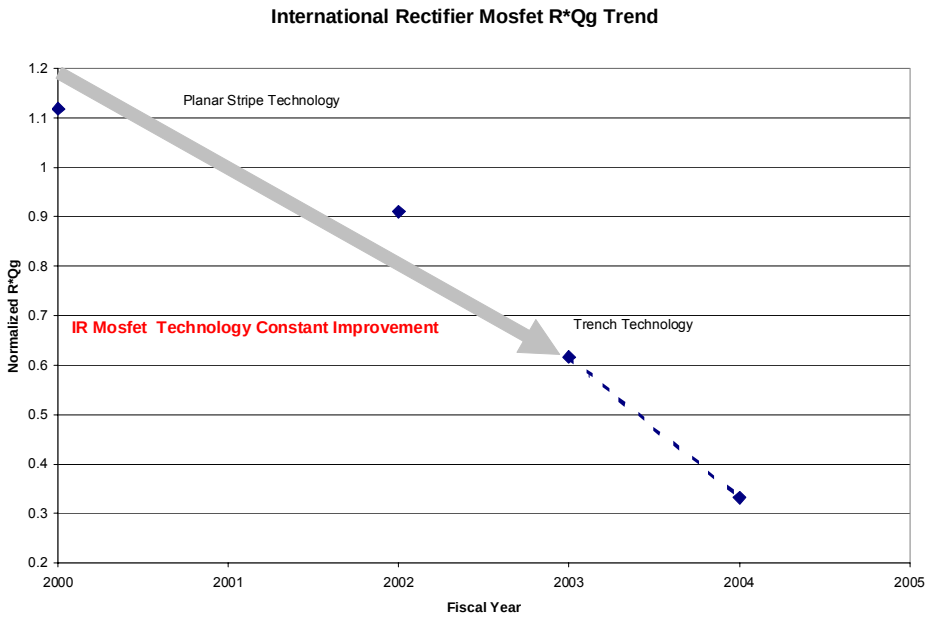
1. MOSFET Technology Trend

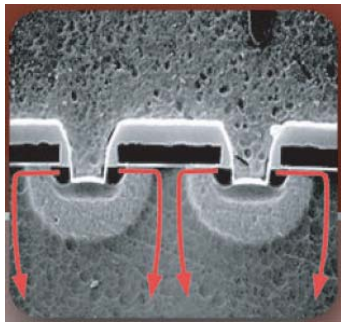
A MOSFET has inherent trade-offs between ON resistance and gate charge, $R_{DS(on)}$ vs Qg. In device design, this translates into Conduction loss vs Switching loss trade-off.

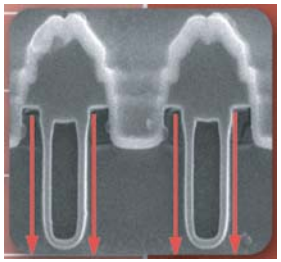
The objective of optimization for Class D applications is to achieve minimal power loss.

Newer platforms show better FOM (Figure of Merit)

➔ This is what makes Class D keep improving!

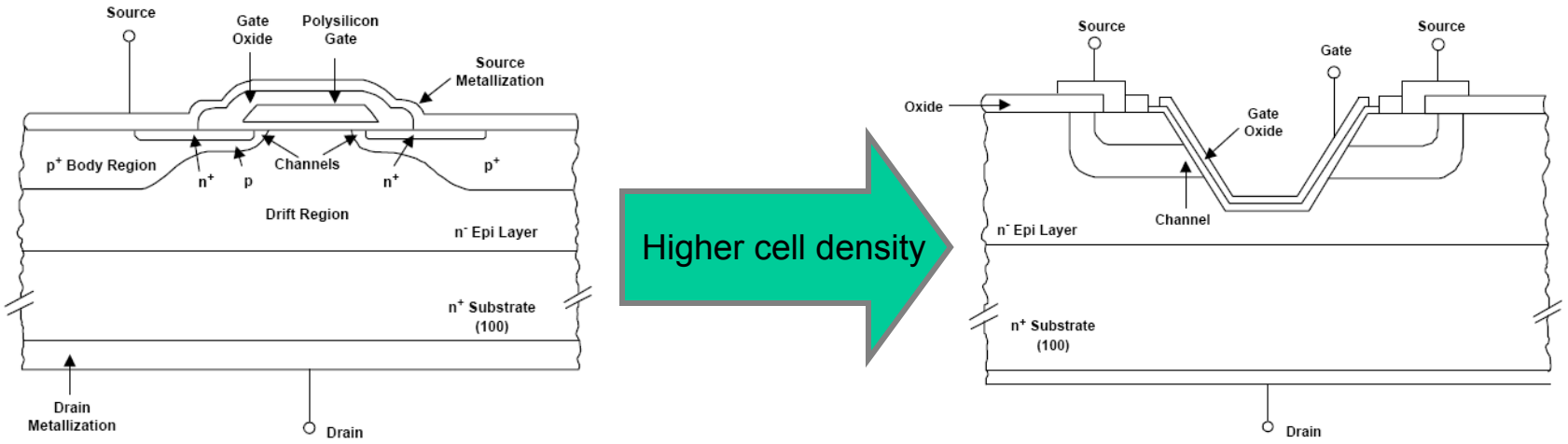






MOSFET Evolution

The latest trench MOSFET technology shows 7 times better figure of merit.



Planar MOSFET Structure

IRF540

100 V

66m ohms

50 nC

$R_{DS(on)}$ x Qg=3300

Trench MOSFET Structure

IRF6665

100 V

53m ohms

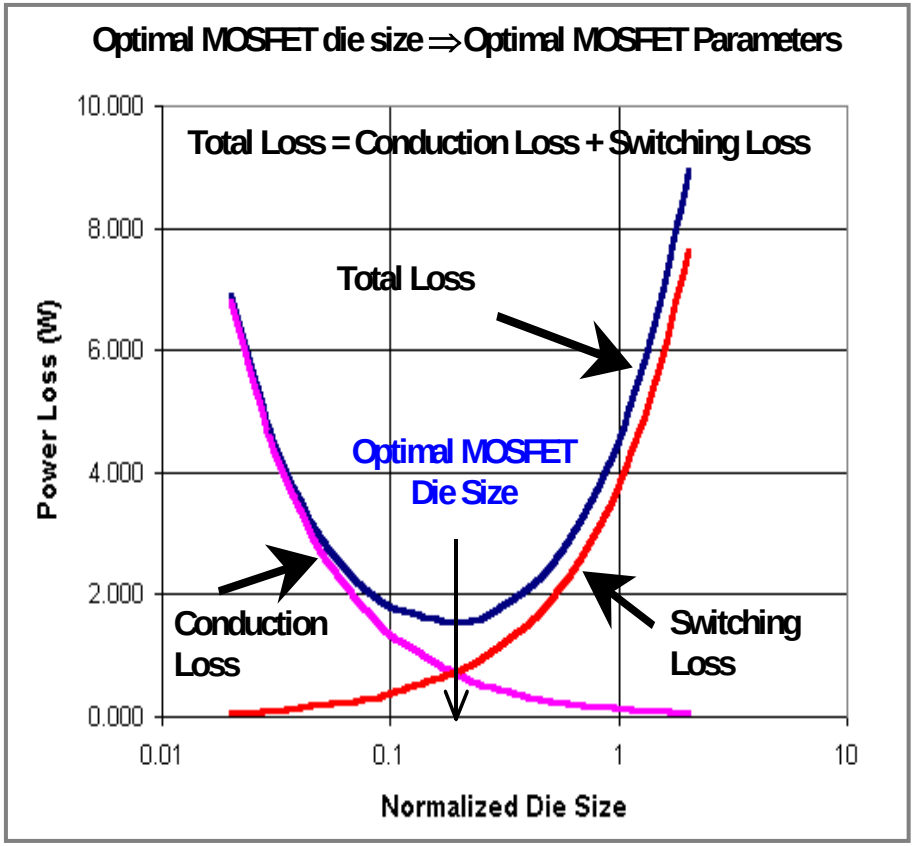
8.4 nC

$R_{DS(on)}$ x Qg=445

Trade-offs in MOSFET Design

There is a best die size for a given output power. Optimum die size for minimal P_{LOSS} depends on load impedance, rated power and switching frequency.

A more advanced platform with better FOM acheives lower P_{LOSS}.



To learn more about MOSFET selection, refer to AN-1070 Class D Amplifier Performance Relationship to MOSFET Parameters.

Importance of Packaging

How the package affects the design?

To utilize benefits from a newer generation MOSFET, new package with reduced stray inductance is necessary.

1. Amplifier size

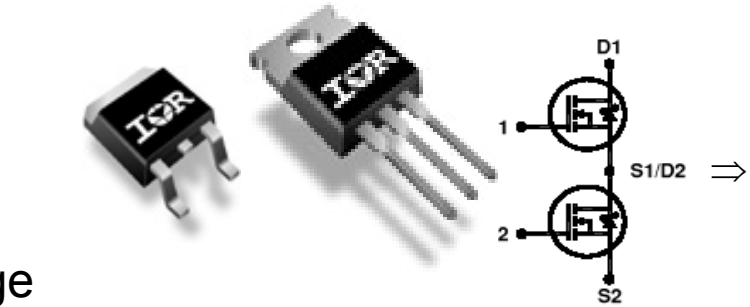
- Increase efficiency
- Increase current capability
- Improve the MOSFET thermal efficiency

2. EMI considerations

- Better control of current and voltage transients

3. Amplifier linearity

- Decrease switching times
- Narrow the MOSFET parameter distribution



TO-220 Full-Pak
5 PIN

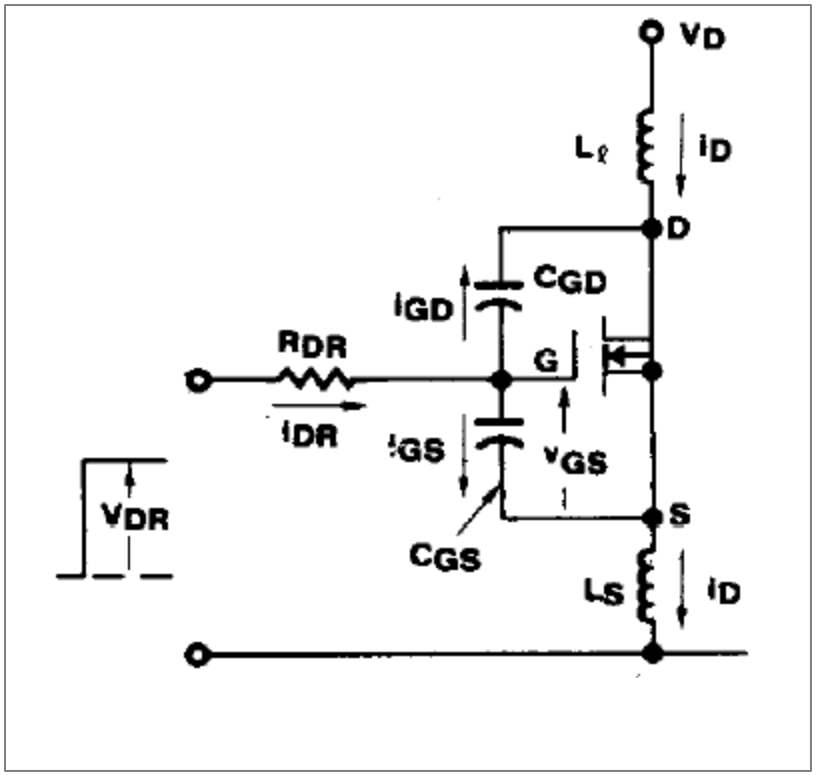
Stray Inductance

A MOSFET has capacitive elements.

Stray inductance is where excessive energy is stored, causing over/under shoots and rings.

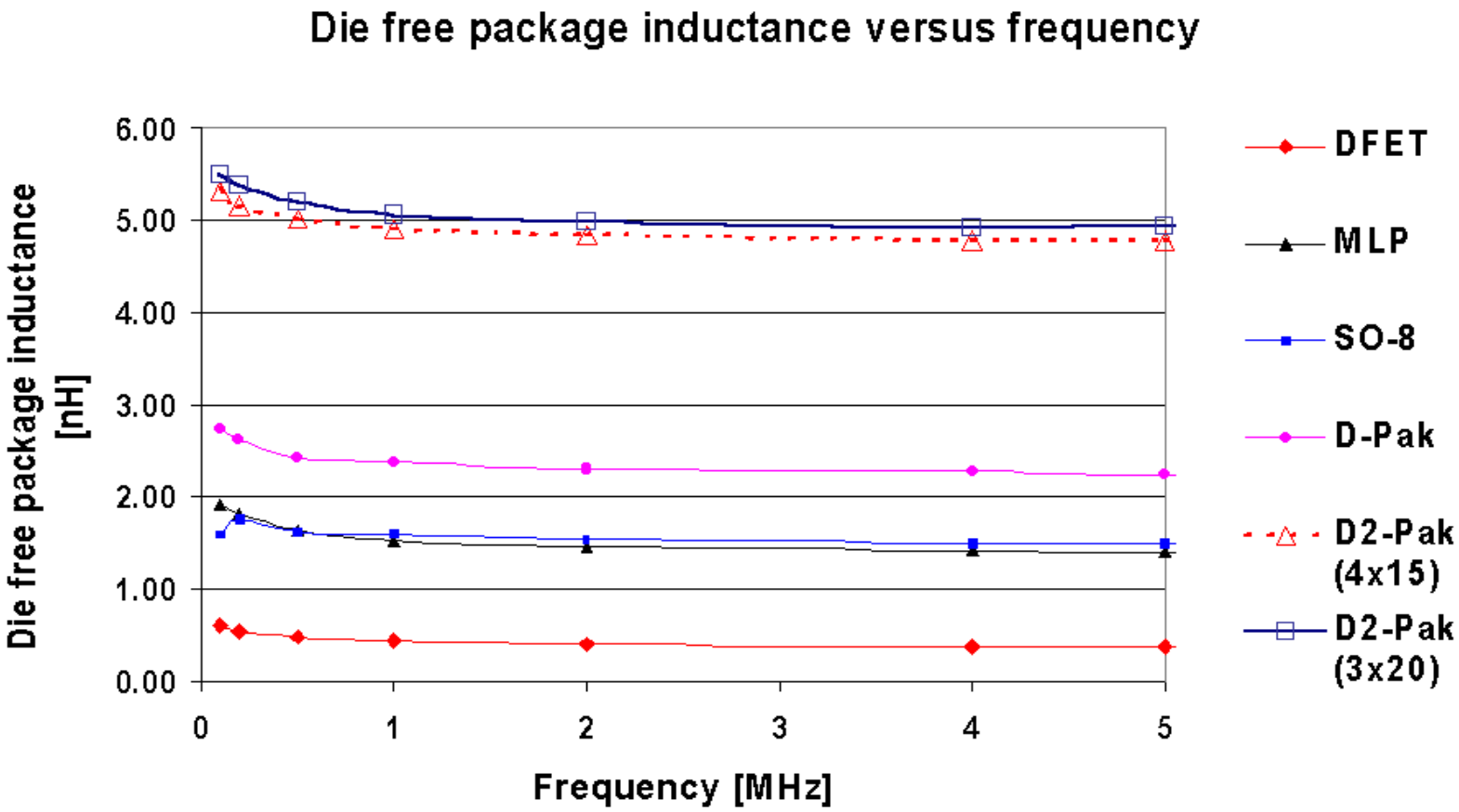
Stray inductance in Source returns feedback voltage to gate, slowing down switching speed significantly.

The smaller the parasitic components the better performance!



To learn more about MOSFET switching behavior, refer to AN-947 Understanding HEXFET Switching Performance.

Package Comparison

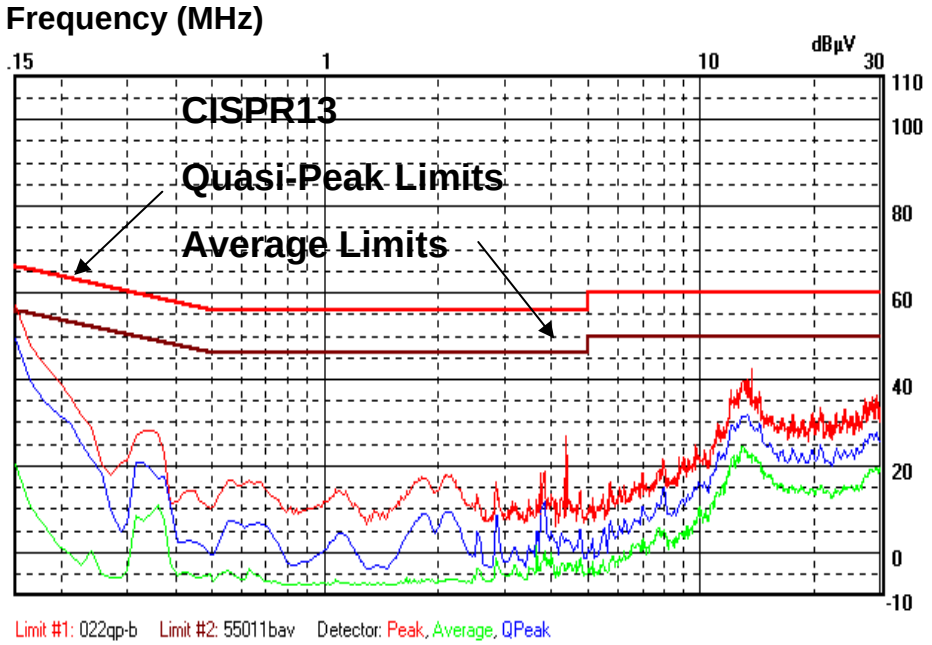


- Lower inductance at frequency than SO-8, D-Pak, MLP and D-Pak
- TO-220 inductance package is ~ 12nH
- DirectFET® is 0.4nH

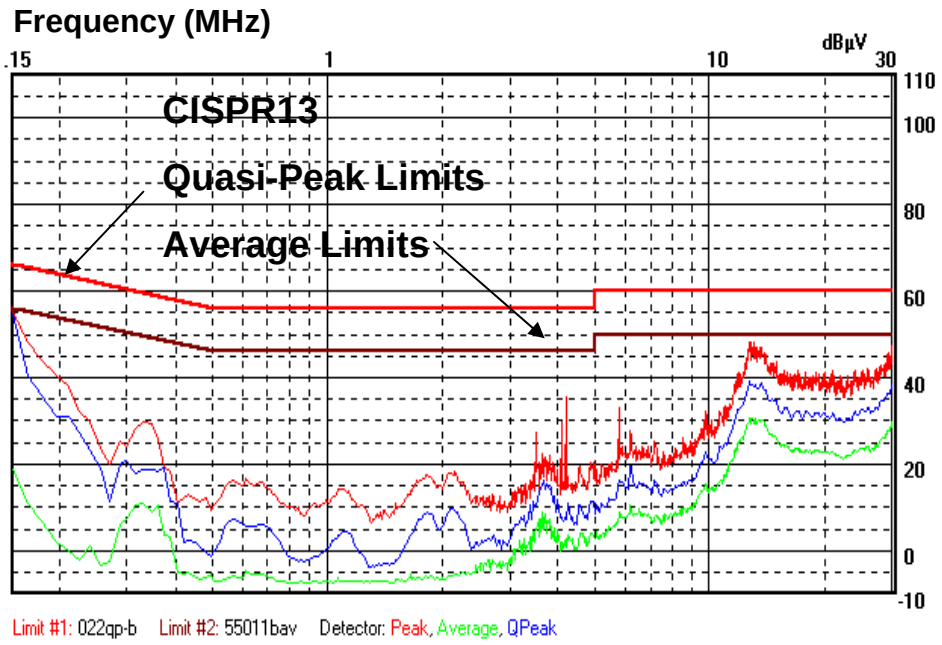
EMI Comparison

- DirectFET® amplifier shows better EMI performance than TO-220 amplifier
- Over 2MHz, DirectFET amplifier shows approximately 9dBuV lower Peak, Quasi-Peak and Average noise than TO-220 amplifier
- Both PCB's meet audio amplifier EMI standards limits (CISPR13)

DirectFET

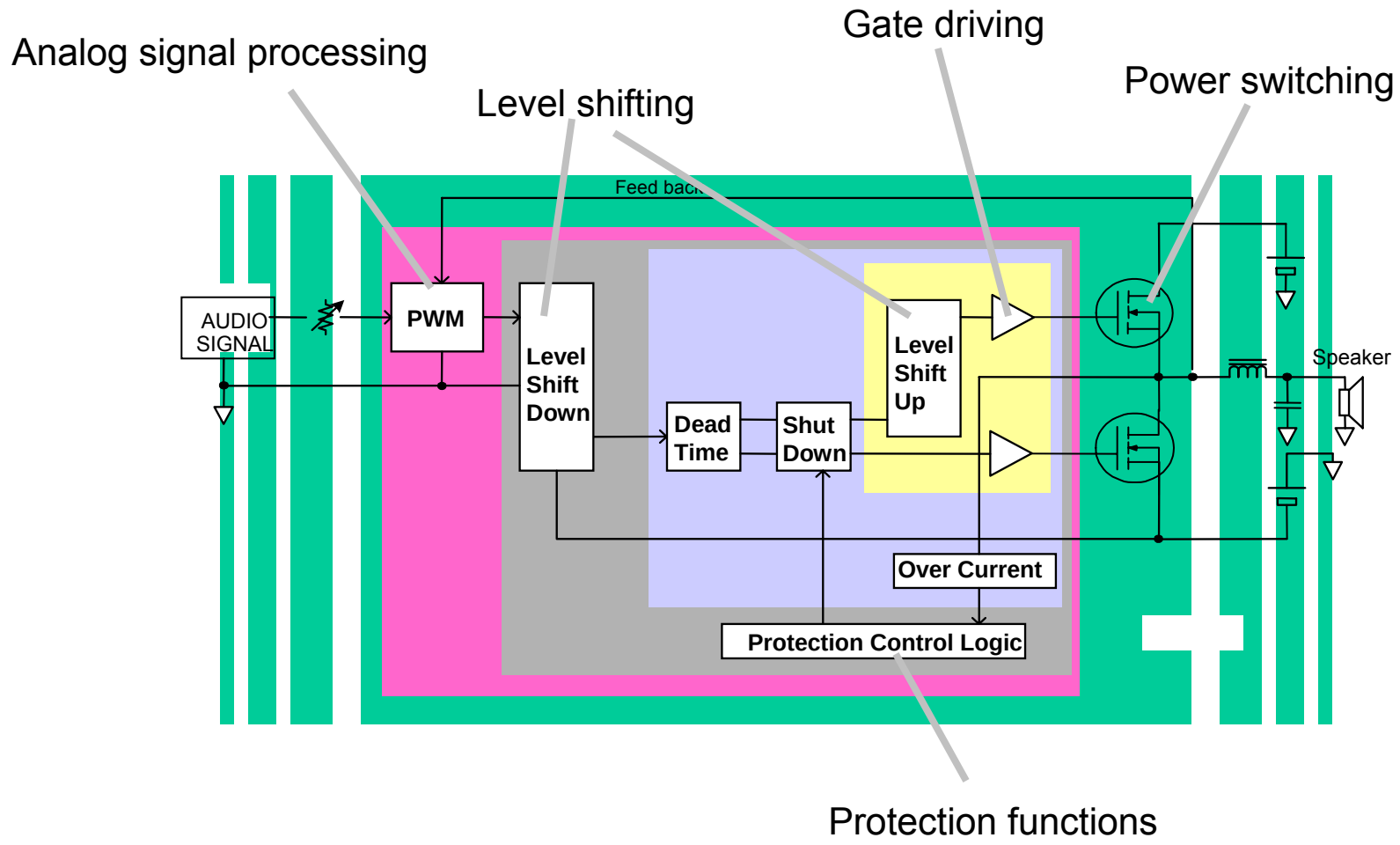


TO-220 (w/DirectFET die)



2: Gate Driver IC Technology Trend

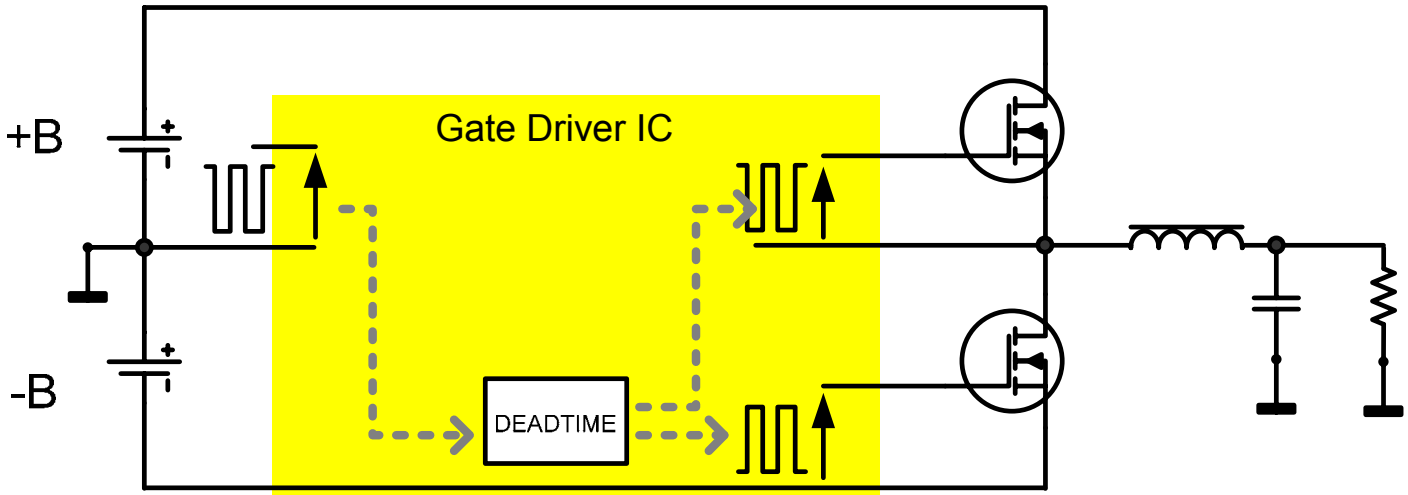
- More integration to realize smaller footprint



What The Gate Driver IC Does?

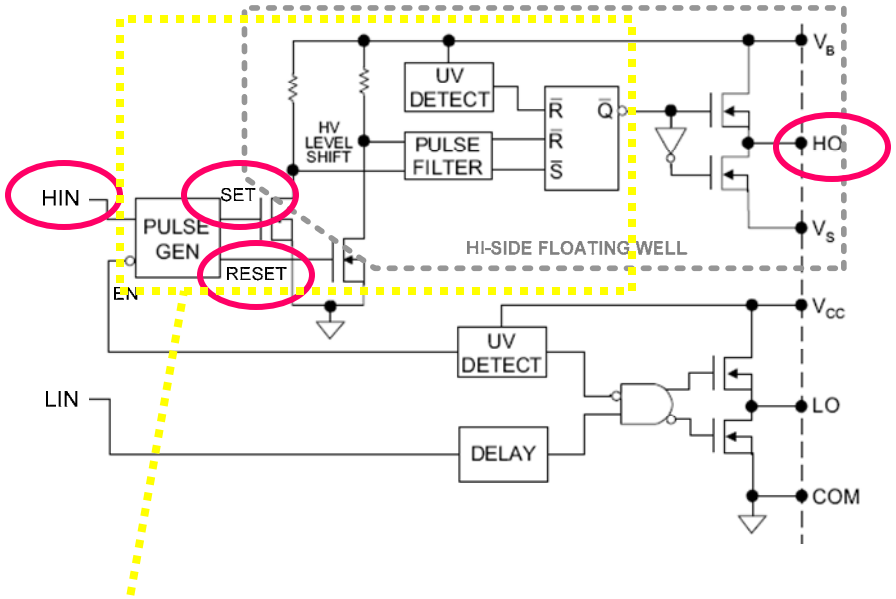
Four Essential Functions in Gate Driver IC

- Level Shift
- Deadtime Generation
- Gate Drive
- Under Voltage Lockout

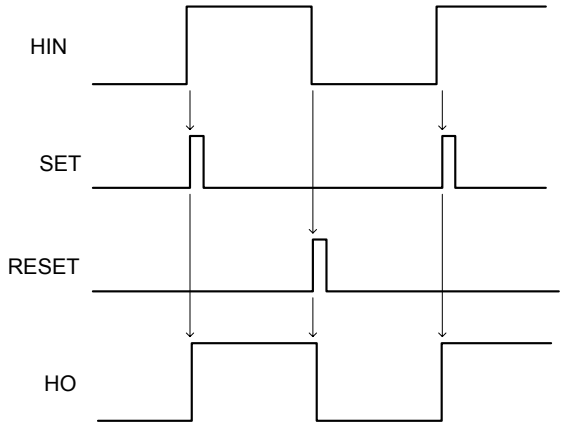


To learn more about High Voltage Gate Driver IC, refer to AN-978 HV Floating MOS-Gate Driver ICs.

How Internal High Voltage Level Shifter Works



Pulse Gen Waveform Example



Operation Principle

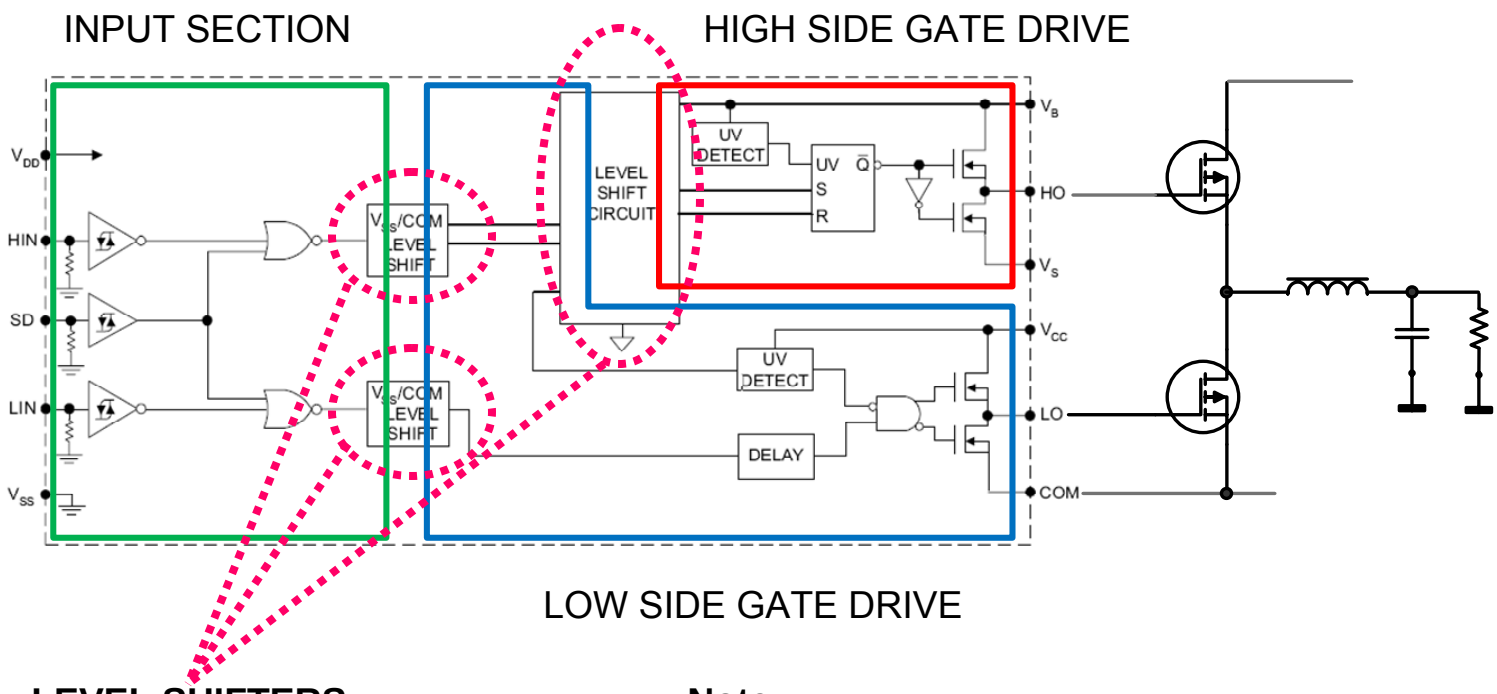
A pair of SET and RESET signals are generated at the PULSE GEN block.

The SET and RESET pulses drive the high voltage MOSFET to send these signals to circuitries in a floating high-side well.

The high-side circuitry reconstructs PWM from SET and RESET pulses.

This method minimizes power dissipation in the high voltage MOSFETs in level shifter.

Floating Well and Noise Isolation



LEVEL SHIFTERS

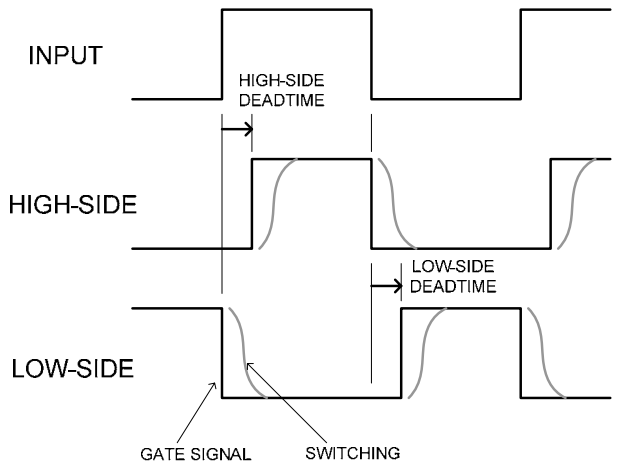
- Translate PWM signal to different voltage potential
- Isolate circuit blocks that are in different voltage potentials

Note

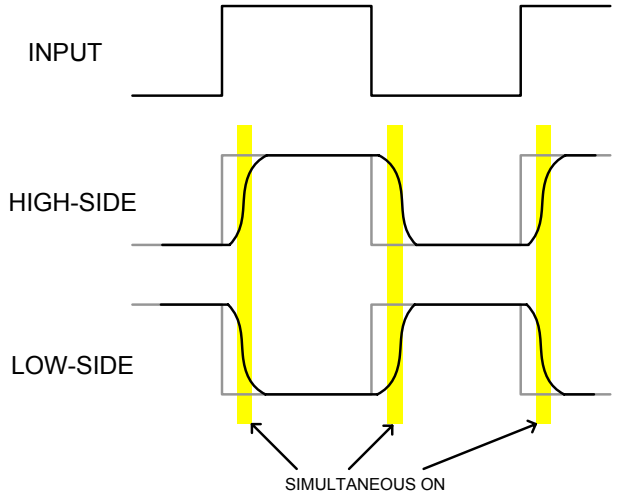
- Level shifter rates supply voltage ranges
- Level shifting is useful to drive high-side the MOSFET whose source is tied to switching node.
- Level shifting blocks switching noise coming into sensitive input section.

Dead-time Generation

With Dead-time



Without Dead-time



Dead-time (or blanking time) is a period of time intentionally inserted in between the ON states of high- and low-side MOSFETs.

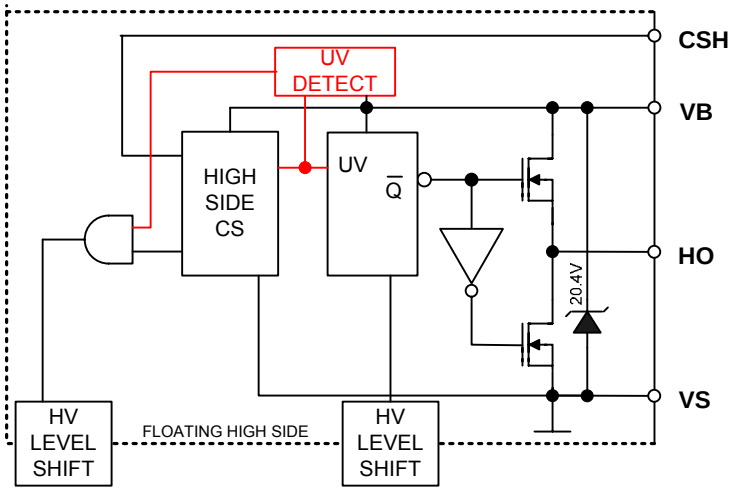
This is necessary because the MOSFET is a capacitive load to the gate driver that delays switching time and causes simultaneous ON.

Lack of dead-time results in lower efficiency, excessive heat and potential thermal failure.

Usually, dead-time is realized by delaying turn on timing.

Under Voltage Lockout

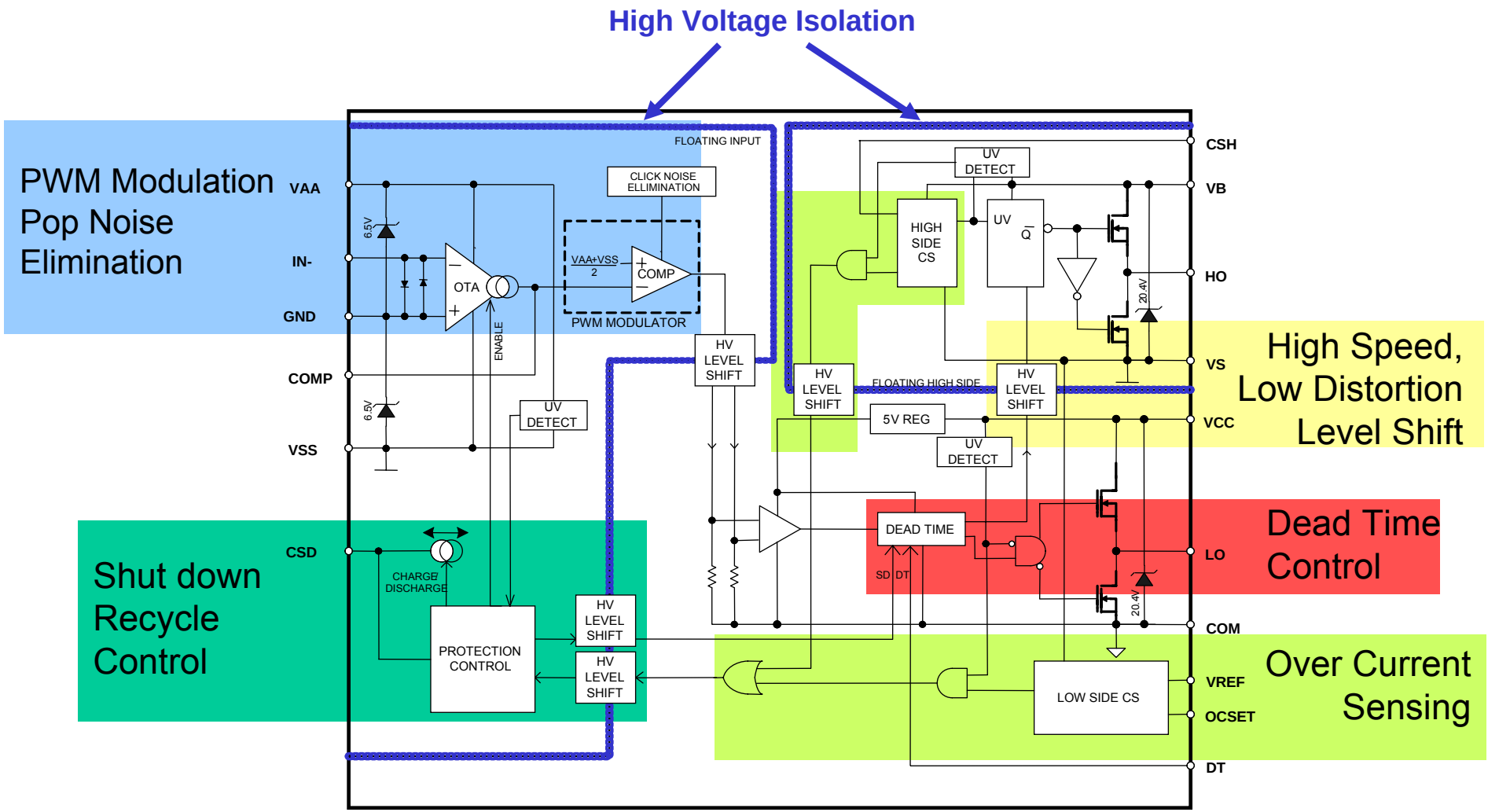
- Under voltage lockout (UVLO) prevents the MOSFET from entering the “half-ON” region when the gate bias voltage is reduced.
- The “half-ON” condition of the MOSFET creates excessive power loss due to increased $R_{DS(on)}$ that could lead to MOSFET failure, therefore must be avoided.



- During the UVLO, gate drive stage keeps HO/LO low in order to prevent unintentional turn-on of the MOSFETs.
- UVLO in V_{CC} resets shutdown logic and causes CSD recycling to start over the power up sequence.
- The IR Class D audio gate driver family is designed to accept any power sequence.

UVLO of VBS shuts down HO and disable high-side current sensing

Inside of High Voltage Gate Driver IRS2092



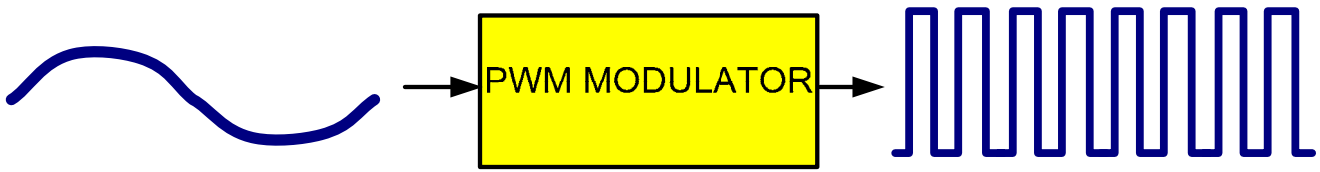
3. PWM and Feedback Technologies

PWM modulator's functions

- Convert analog or digital audio signal (PCM) to PWM that has reasonable switching frequency for power MOSFET
- Error corrections to improve audio performance

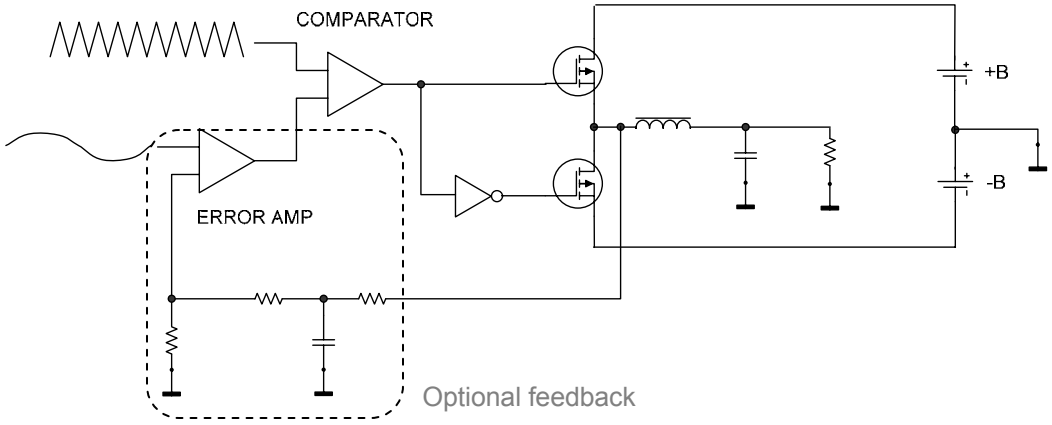
Demands

- Feedback to reduce DC offset, distortion and noise floor
- Larger loop gain for lower distortion, higher power supply rejection ratio (PSRR)
- Post filter feedback for higher damping factor
- Switching frequency control for reduced EMI



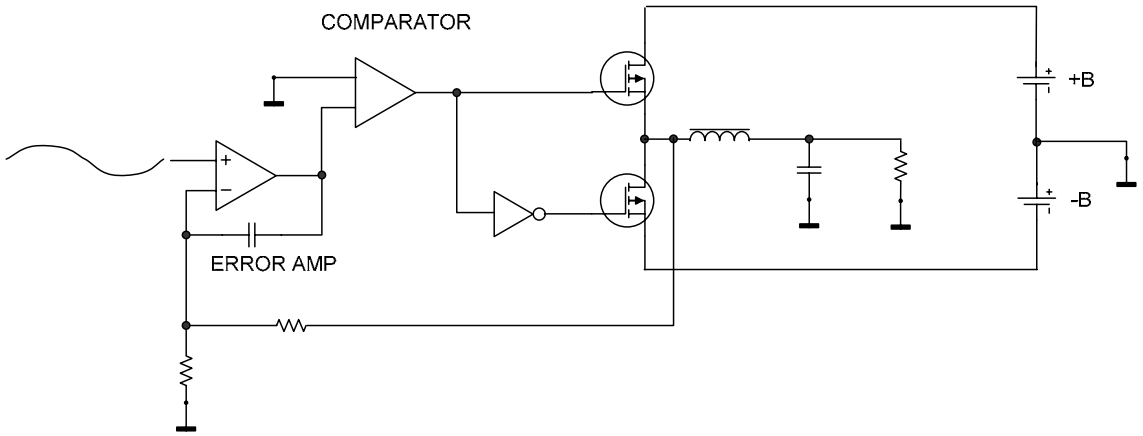
Natural PWM vs. Self Oscillating PWM

Natural PWM



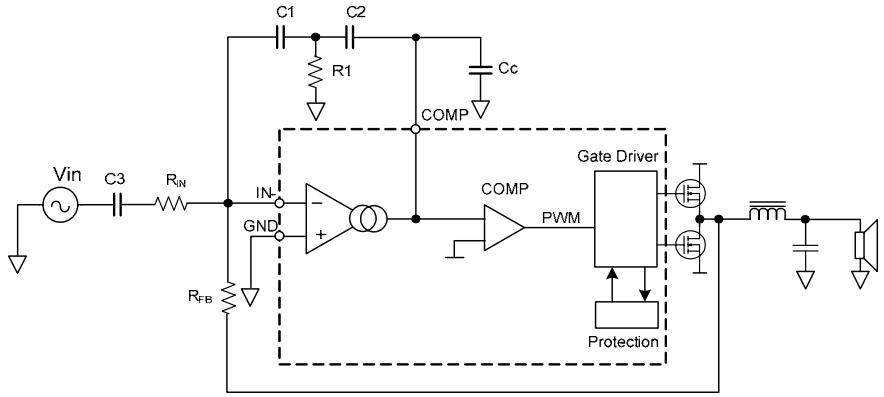
- Open loop or closed loop
- Fixed frequency

Self-oscillating PWM

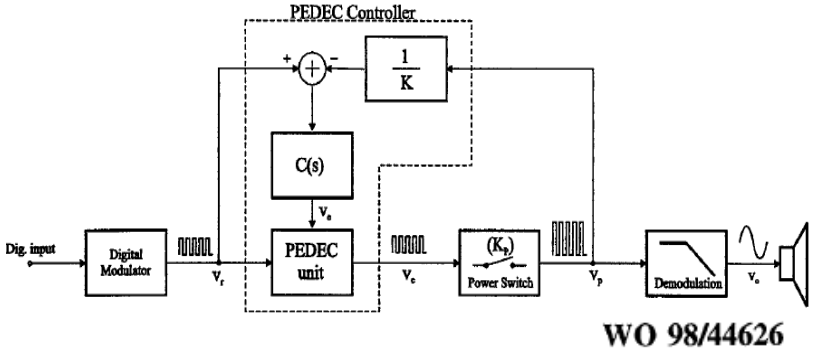


- Closed loop
- Frequency changes with modulation
- High loop gain
- Fewer components

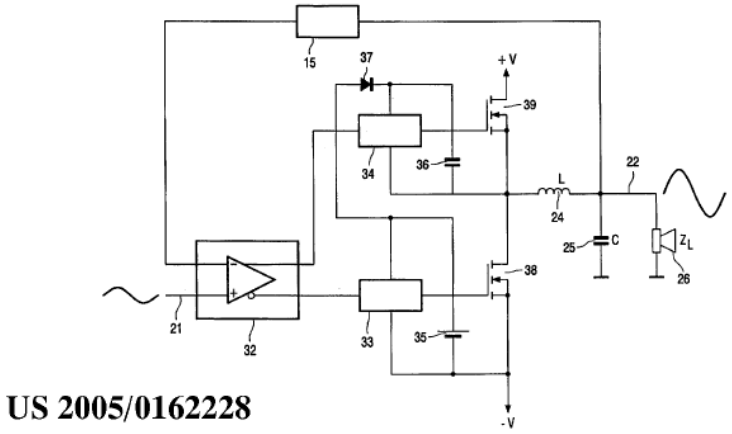
Modern PWM Topologies



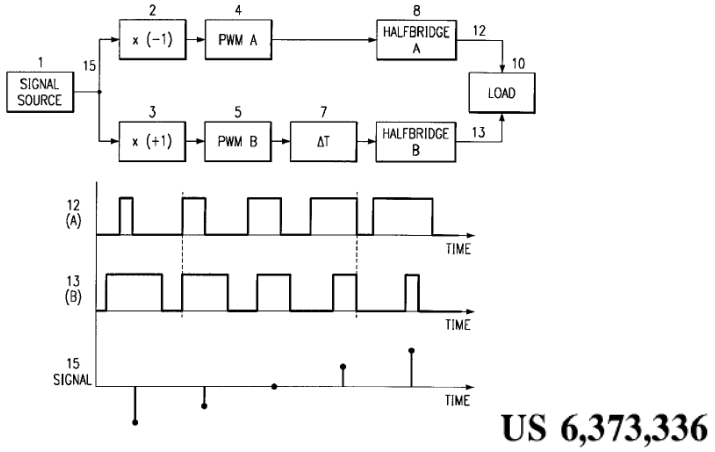
Self-oscillating PWM with 2nd order integration



Self-oscillating PWM with pulse width control



Global feedback from speaker output

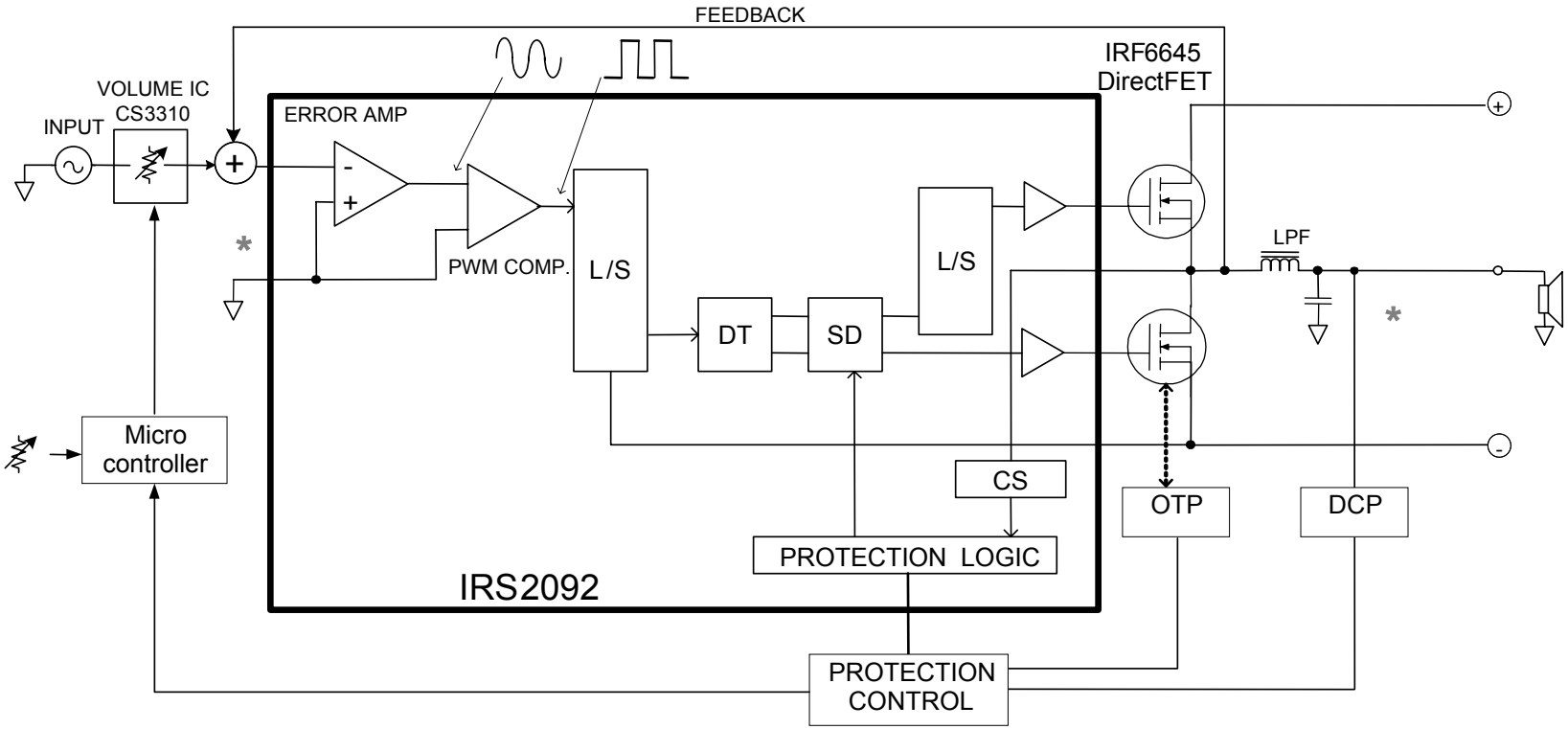


Inductor-less PWM

IRAUDAMP5 Functional Block Diagram

Typical IR audio evaluation board based on self-oscillating PWM with 2nd order integration

*



Chapter 3:
Identifying Problems ~ Performance Measurement of Class D Amplifier

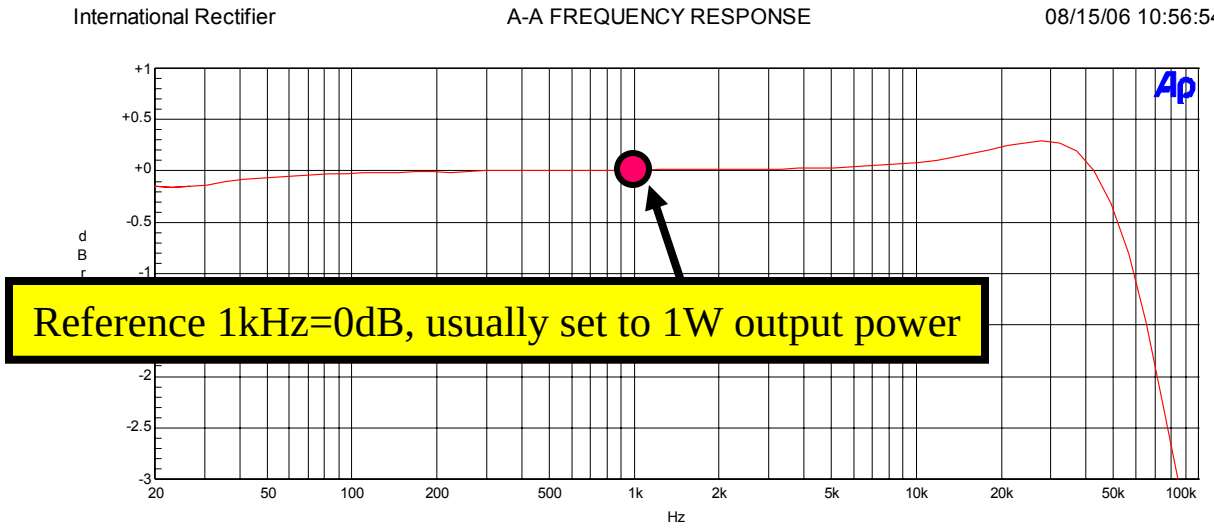
Identifying Problems

- Proper audio performance measurement is crucial to identify potential problems.
- Frequency response and THD+N are the minimum basic measure of audio performance.

Problem	Possible Causes
Low frequency response	Audio input, feedback network
High frequency response	Audio input, feedback network, LPF design
High harmonic distortion	Shoot-through, dead-time, switching noise coupling
High noise floor	Analog input, switching noise coupling

1. Frequency Response

- Use resistive dummy load.
- Set reference voltage level to 1W output power at 1kHz.
- Sweep sinusoidal signal from 20Hz to 100kHz.
- Take frequency response with various load impedances and without loading.

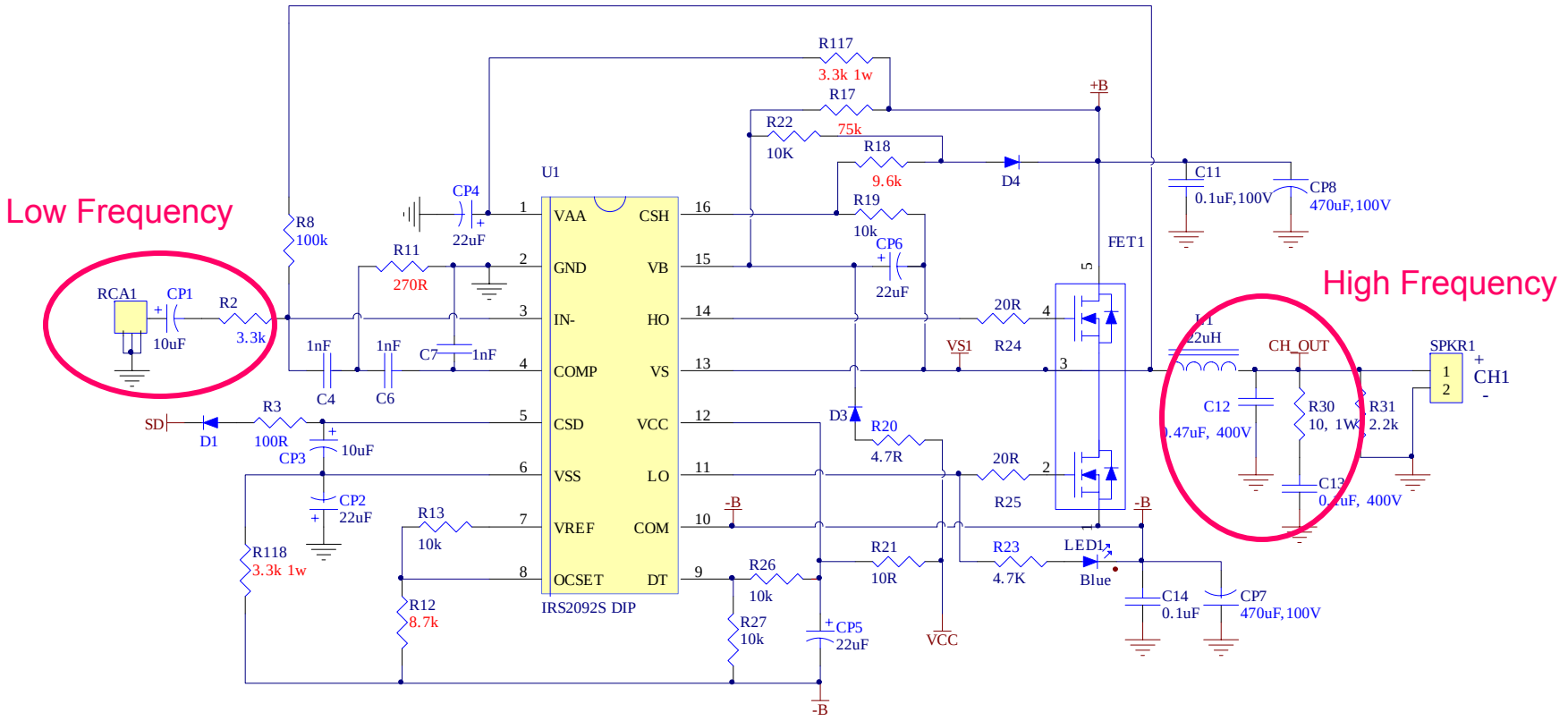


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Anlr.Level A	Left	8Ohm, 1W, 80kHz BW

Frequency Response from 20k to 20 Hz. F4 first to set 0 dBr at 1kHz. The 2 Ch Ampl Function Reading meter BW is set to <10 Hz & >500kHz so the bandwidth is the same as the Level meter. Optimize for detail.

A-A FREQ RESP.at2

Check for..


Low Frequency
High Frequency
U1
IRS2092S DIP
VAA
GND
IN-
COMP
CSD
VSS
VREF
OCSET
CSH
VB
HO
VS
VCC
LO
COM
DT
R117
3.3k 1w
R17
R22
75k
10K
R18
9.6k
R19
10k
D4
+B
C11
0.1uF,100V
CP8
470uF,100V
FET1
CP4
22uF
R8
100k
R11
270R
CP6
22uF
RCA1
CP1
10uF
R2
3.3k
1nF
C4
1nF
C6
C7
1nF
20R
R24
VS1
L1
22uH
CH_OUT
SPKR1
CH1
C12
0.47uF, 400V
R30
10, 1W
R31
2.2k
C13
0.47uF, 400V
SD
D1
R3
100R
CP3
10uF
D3
R20
4.7R
20R
R25
-B
CP2
22uF
R13
10k
R118
3.3k 1w
R12
8.7k
R21
10R
R23
4.7K
LED1
Blue
R26
10k
R27
10k
CP5
22uF
VCC
C14
0.1uF
CP7
470uF,100V

2: THD+N

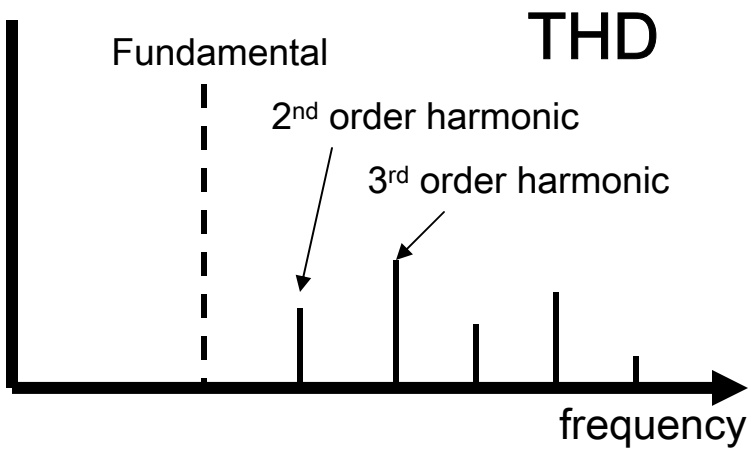
- THD+N is a sum of harmonic distortion components and noise, i.e. anything except fundamental spectrum.

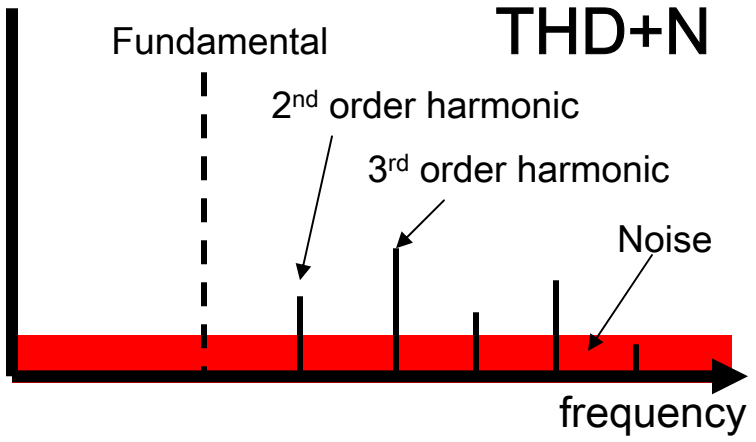
- **THD** is a measure of linearity.

➔ Refer to Chapter 4

- **Noise** is a measure of added errors not depending on the input signal

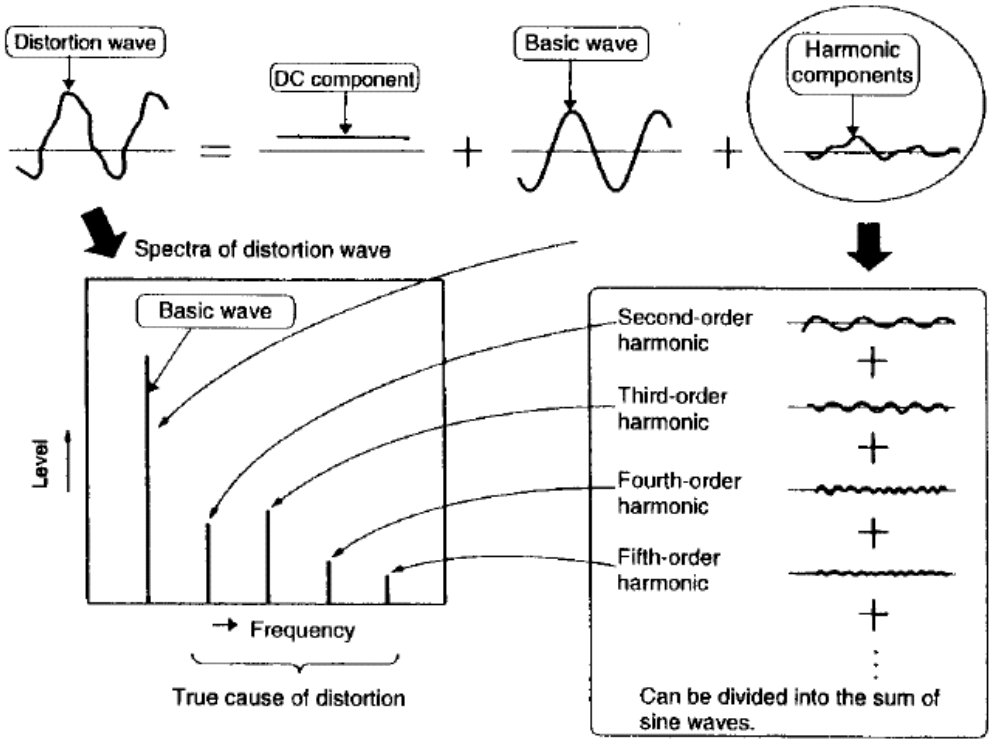
➔ Refer to Chapter 5





What is Distortion?

- THD is a simple way to measure non-linearity of the amplifier.
- If the amplifier is not linear, it generates harmonics.



Any repetitive waveforms can be expressed as a sum of sinusoidal signal as

$$V_o = dc + \sum_{n=1}^{\infty} A_n \bullet \sin(nwt + \theta_n)$$

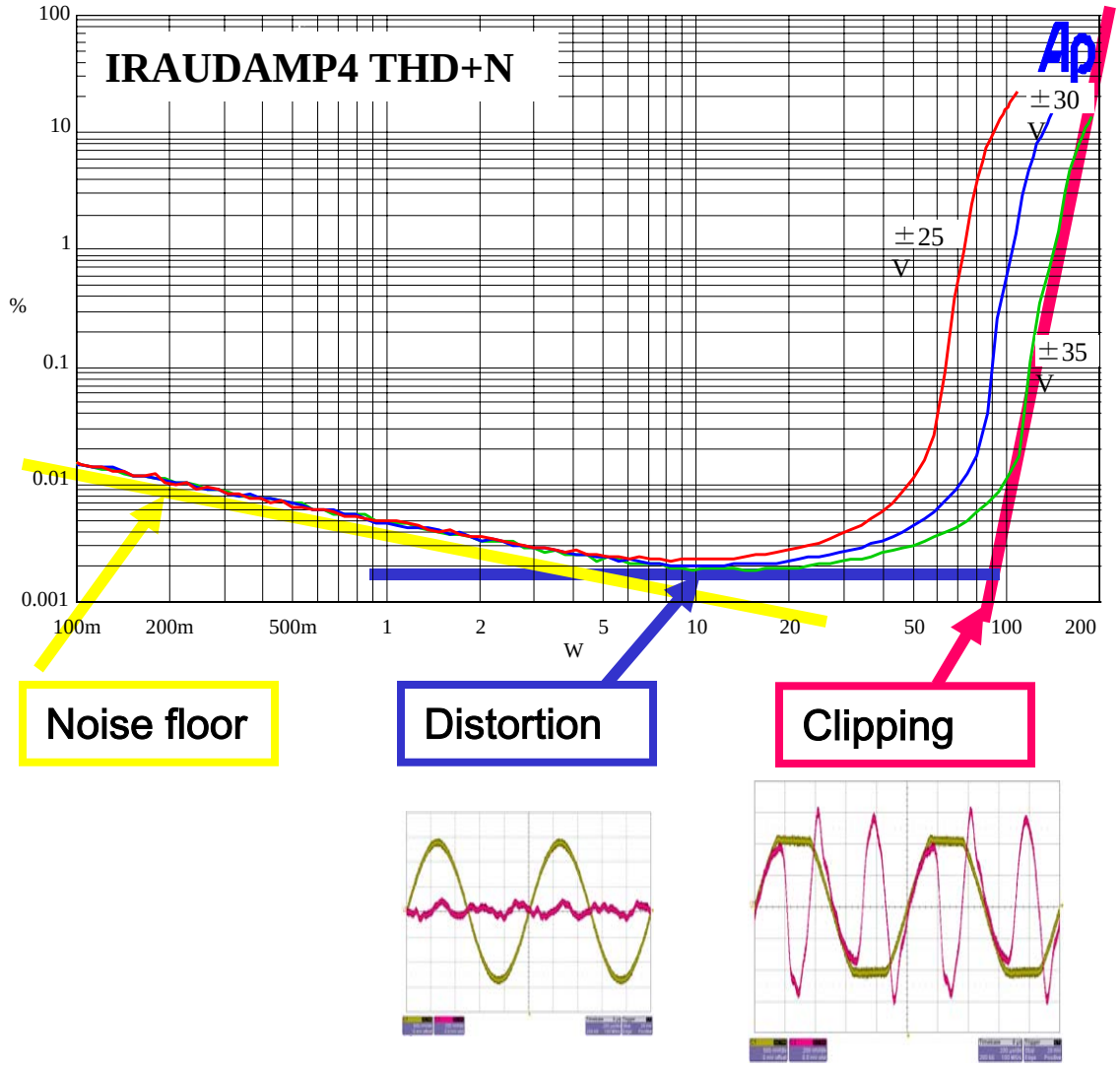
Harmonic distortion is a ratio of rms value of the harmonic component and the original waveform.

$$HDn = A_n / A_1$$

Total harmonic distortion is a ratio of rms value of sum of the all harmonic component and the original waveform.

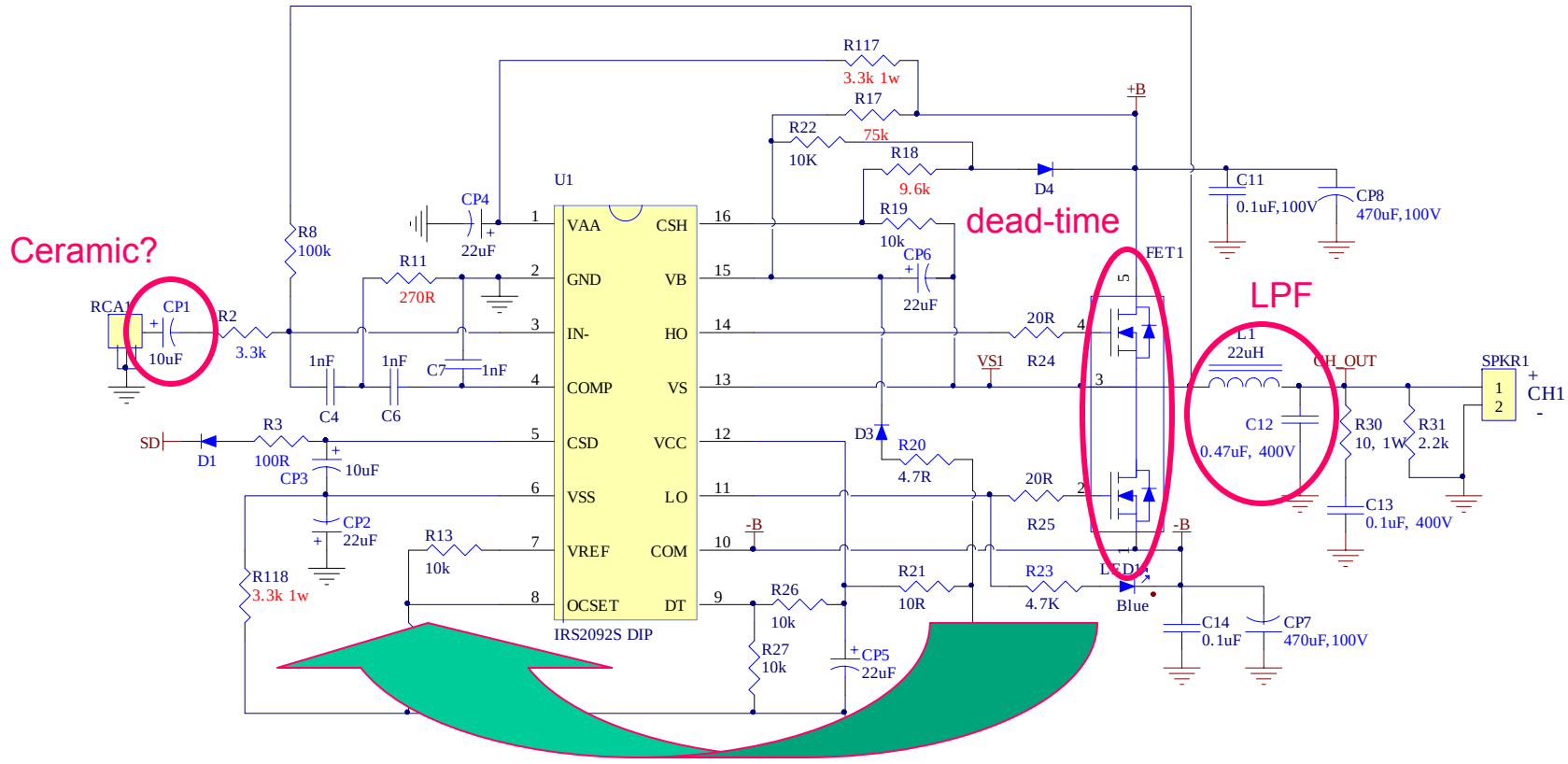
$$THD = \sqrt{\left(\sum_{n=2}^{\infty} HDn^2\right)}$$

How to Read THD+N vs. Power

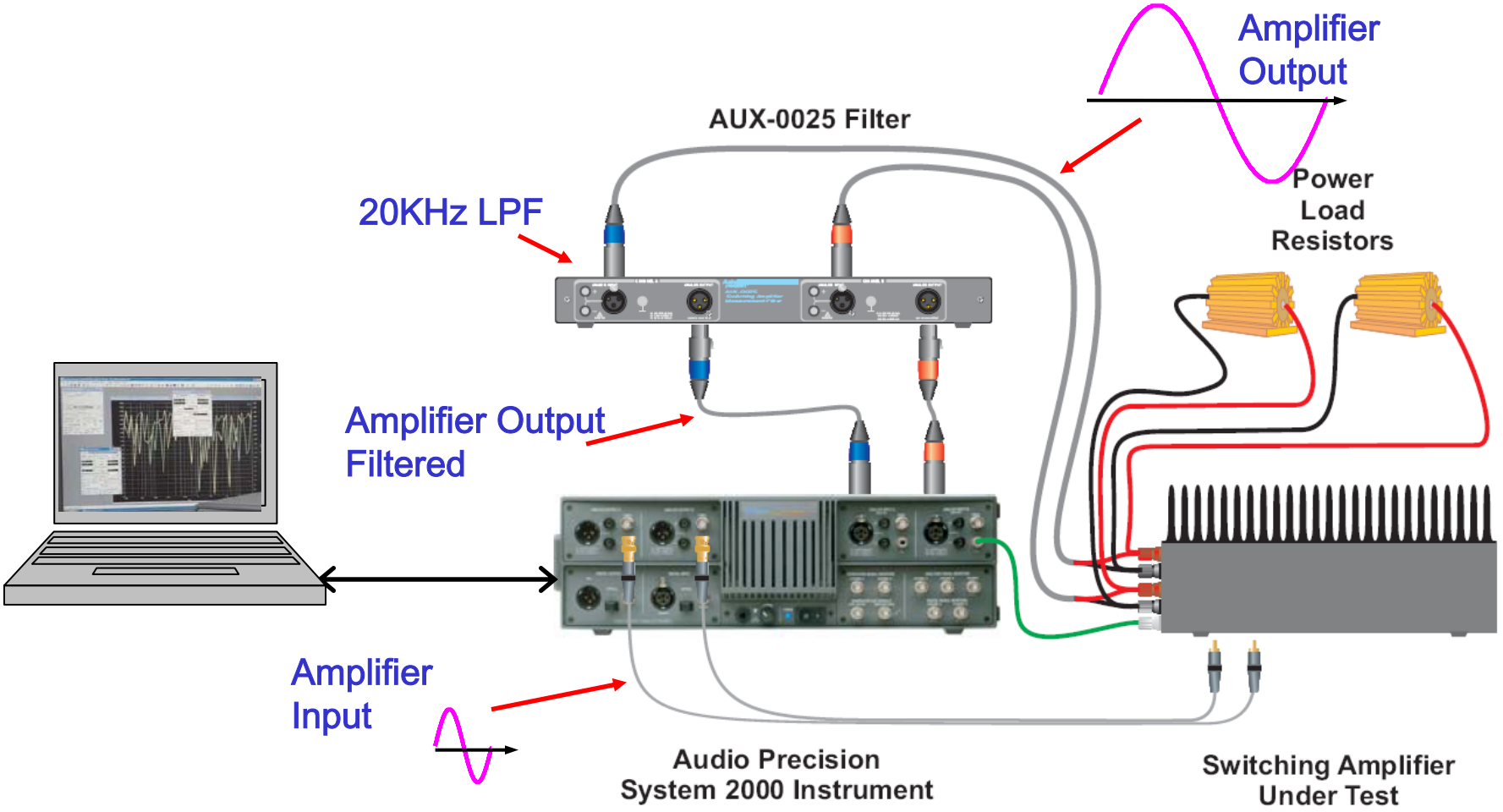


- THD+N vs. Power spells out noise floor, distortion and output power in a shot.
- Noise floor dominant part has 20dB/dec slope.
- Reading above noise floor slope is dominated by harmonic distortion.
- To trouble shoot, better to start with single channel operation.

Check for..

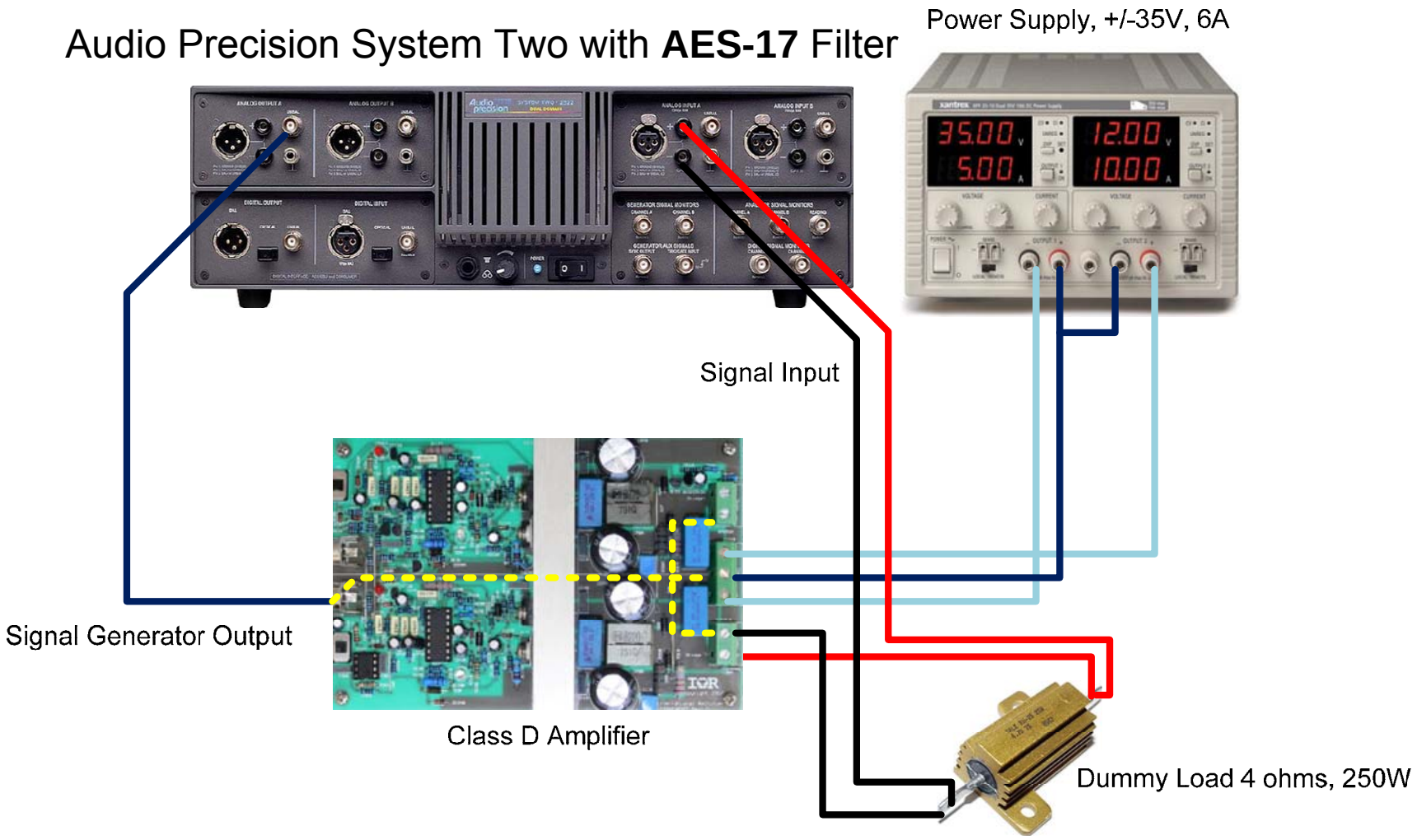

Ceramic?
dead-time
LPF
Switching noise coupling
U1
IRS2092S DIP
VAA
GND
IN-
COMP
CSD
VSS
VREF
OCSET
CSH
VB
HO
VS
VCC
LO
COM
DT
FET1
RCA1
CP1
10uF
R2
3.3k
R8
100k
R11
270R
CP4
22uF
1nF
C4
C6
C7
SD
D1
R3
100R
CP3
CP2
R118
3.3k 1w
R13
10k
R117
3.3k 1w
R17
R22
75k
10K
R18
9.6k
D4
R19
10k
CP6
R24
20R
D3
R20
4.7R
R25
R21
10R
R23
4.7K
LED1
Blue
R26
R27
CP5
+B
-B
C11
0.1uF,100V
CP8
470uF,100V
L1
22uH
C12
0.47uF, 400V
CH_OUT
R30
10, 1W
R31
2.2k
C13
0.1uF, 400V
SPKR1
CH1
C14
0.1uF
CP7
470uF,100V

Audio Measurement Setup



For more information on Class D audio measurement, refer to white paper, Measuring Switch-mode Power Amplifiers by Bruce Hofer, from //ap.com

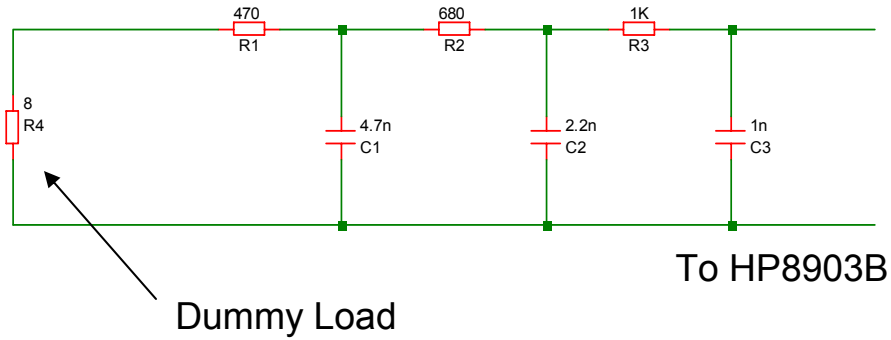
Audio Measurement Setup with IRAUDAMP7D



AP Substitute

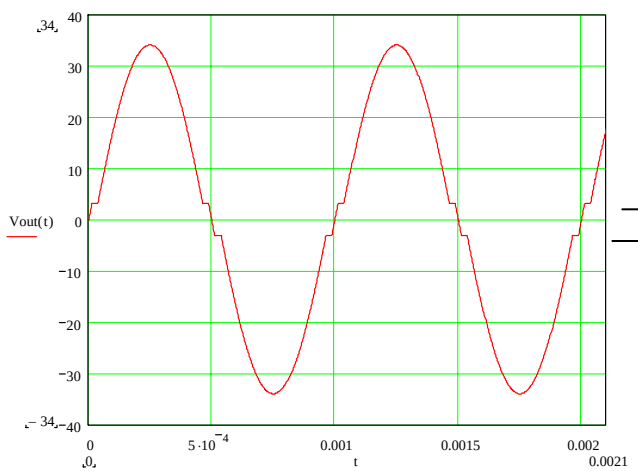
- Old audio analyzers are not designed to tolerate high frequency noise that is from carrier signal residual from a Class D amplifier.
- Place a 3rd order LPF to remove the switching carrier ingredients in front of the audio analyzer
- Check measurements are correct by changing scaling range manually

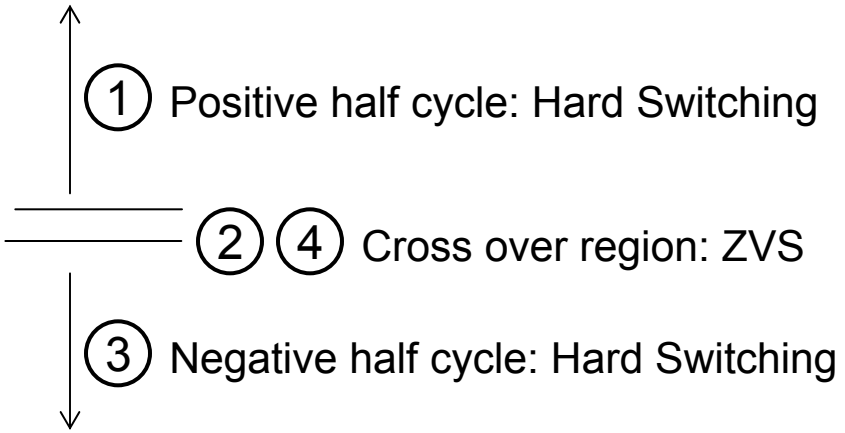
An Example of an additional pre-LPF for HP8903B



Chapter 4:
Reducing Distortion ~dead-time ~ LPF Designs

Trade-off 1: Dead-time and Distortion



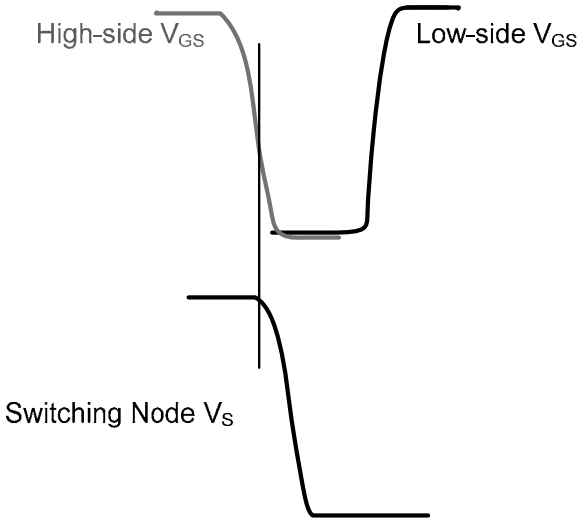


- Dead-time reduces volt-second therefore voltage gain.
- There is a region that dead-time does not affect around zero crossing (regions 2 and 4).
- The smaller the dead-time, the lower the distortion.
- Too narrow dead-time could cause shoot-through from unit-to-unit, temperature and production variations, that could seriously affect product reliability.
- Audio performance and reliability is NOT a trade-off.

Gate Drive and Switching Output

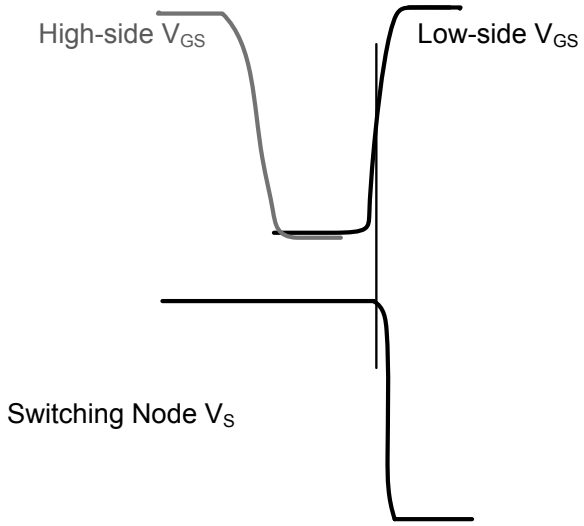
ZVS Region

Turning off of the previous MOSFET dictates transition in switching waveform.

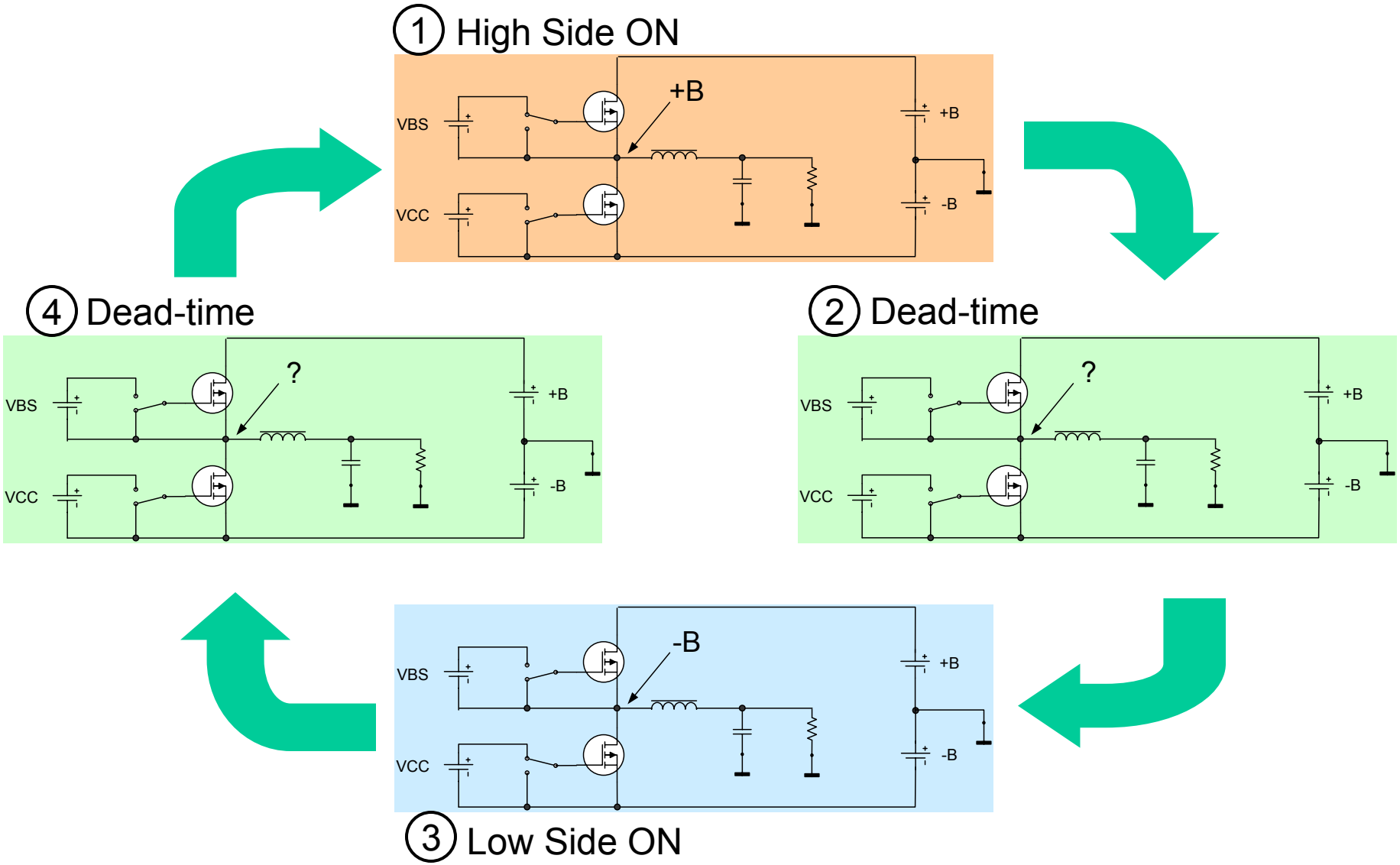


Hard Switching Region

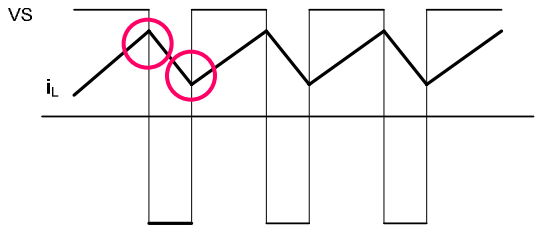
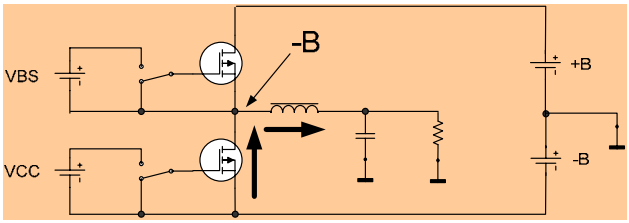
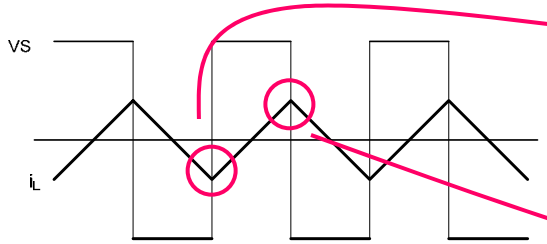
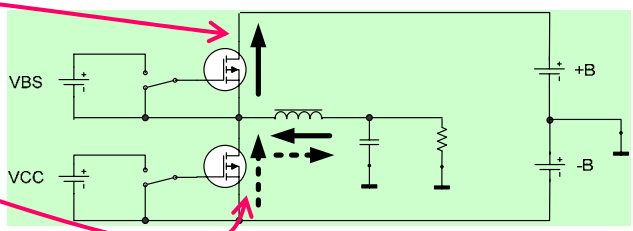
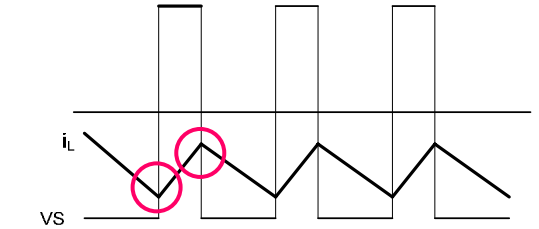
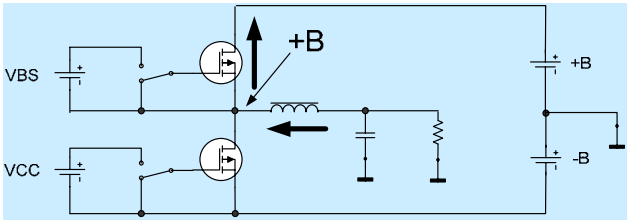
Turning on dictates output switching waveform.



PWM Switching Cycle



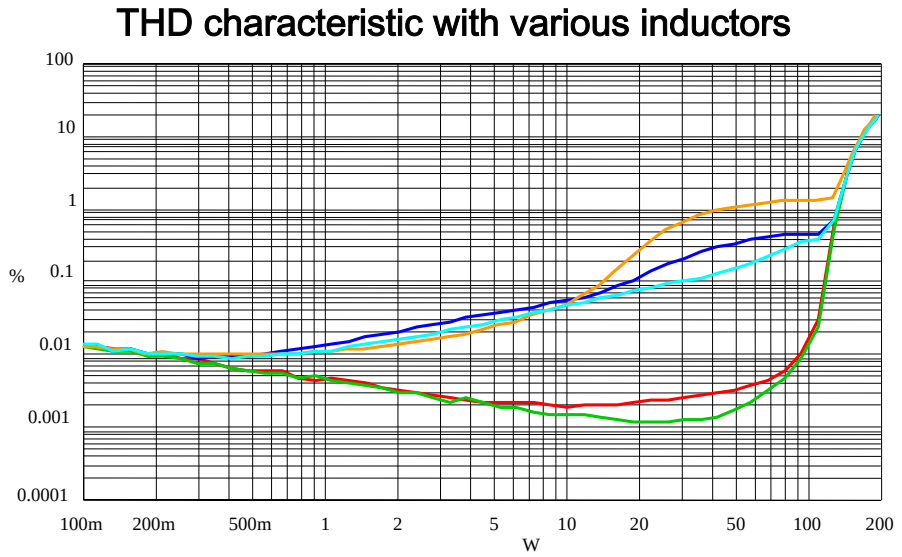
During Dead-time

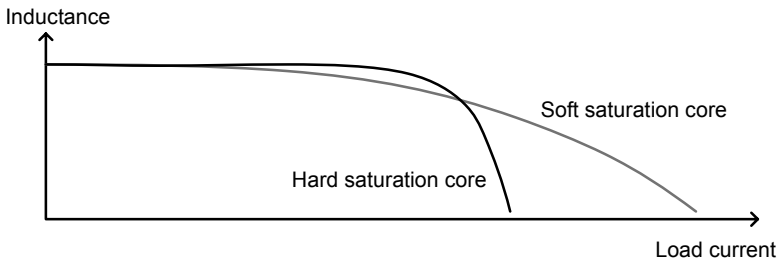
1			• Polarity of I_L is always toward the load • V_S follows high side switch status
2 4			• Polarity of I_L alternates • VS follows turning off edges of both high and low sides • ZVS ➔ No influence from dead-time insertion
3			• Polarity of I_L is always toward the amp • V_S follows low side switch status

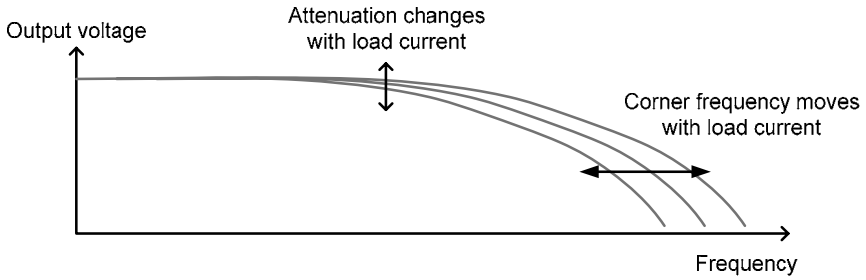
Note: Dead-time insertion reduces volt-second of V_S. Dead-time inserted in the rising edge of the high side affects the operating region 1. Dead-time inserted in the rising edge of the low side affects the operating region 3. As a result, output voltage gets lower than it should be, causing non-linearity in the output stage.

Trade-off 2: Inductor and Distortion

- The quality of the output inductor is crucial to achieve not only the target audio performance but also efficiency.
- Inductance changes with load current, which causes distortion.
- Core saturation increase inductor ripple significantly that can trigger over current protection.







LPF Design

- Set corner frequency according to the bandwidth requirement.
- Design LC-LPF with Q=0.7 for a nominal load impedance to attain flat frequency response.

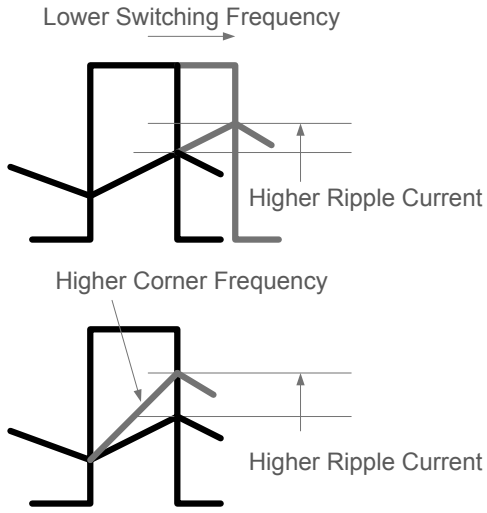
Note that

- The higher the corner frequency the higher the switching carrier leakage
- The lower the corner frequency the bigger the inductance size

Inductance and inductor ripple

$$I_{L\,PP} = \frac{Vbus}{L \cdot f_{SW}}$$

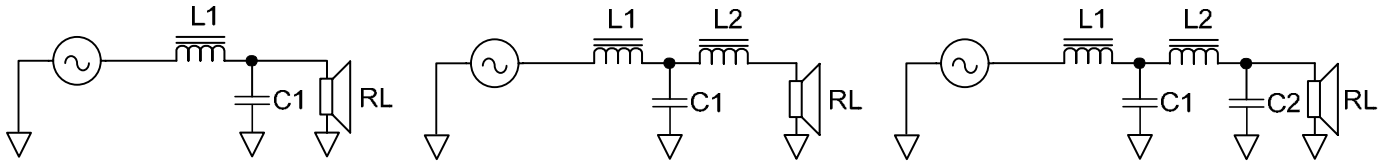
Inductor ripple current dictates ZVS region



LPF Design

1. Decide the order of the filter based on the attenuation of the switching frequency given by:

$$A_t = 10 \cdot \log\left\{1 + \left(\frac{f}{f_C}\right)^{2N}\right\}$$



2nd order LPF　　3rd order LPF　　4th order LPF

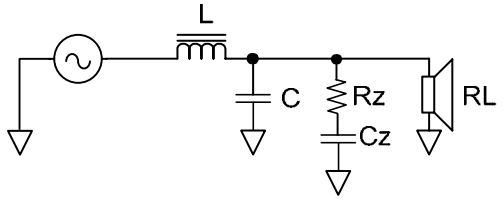
2. Design Butterworth filter

$$L_n = \frac{R_L}{2 \cdot \pi \cdot f_C} Lk_n$$

$$C_n = \frac{Ck_n}{2 \cdot \pi \cdot f_C \cdot R_L}$$

# of Order	Lk1	Ck1	Lk2	Ck2
2	1.414214	0.707107	-	-
3	1.5000	1.3333	0.5000	-
4	1.530734	1.577161	1.082392	0.382683

3. Design Zobel network



Choosing Inductor for LPF

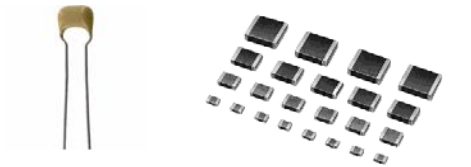
	**Air Coil**	**Large, High DCR, Low distortion, Leakage flux**
 	**Drum Core** **(Ferrite, Open Circuit)**	**Small, Leakage Flux, Low DCR**
  	**Drum Core** **(Ferrite, Closed Circuit)**	**Small, Hard saturation, Low DCR**
	**Toroidal Core** **(Iron Powder)**	**Soft saturation, Lower iron loss**

NOTE

- Ferrite core is suitable for smaller size
- Iron powder is suitable for high power

- Determine I_{RMS} rating for temperature rise condition with 1/8 rated power
- Determine peak current (I_{SAT}) based on maximum load current

Choosing Capacitor for LPF

	**Polyester film, winding**	**Small, High ESR**
	**Ceramic**	**High dielectric type has large distortion, lower AC ratings**
	**Polyester, non-inductive**	**Small, lower AC voltage rating**
	**Polypropylene, non-inductive**	**Low dissipation factor, large size, low distortion**

NOTE

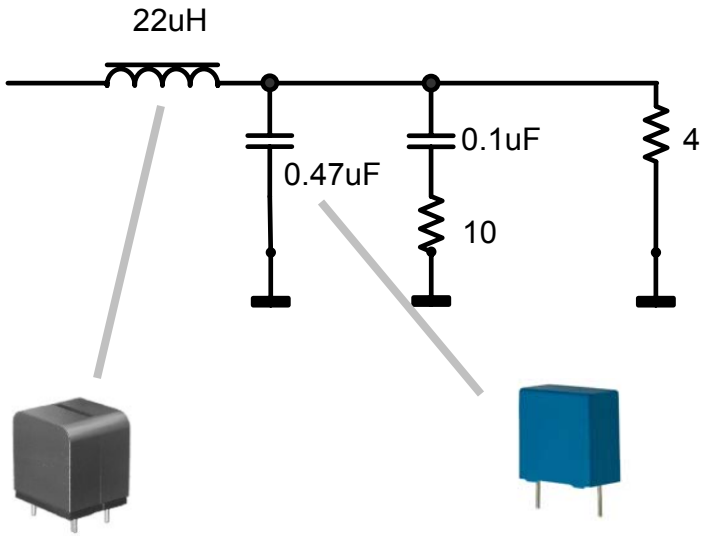
- Do not use winding structure types. Use stacked structure.
- Check AC voltage ratings at highest audio frequency.

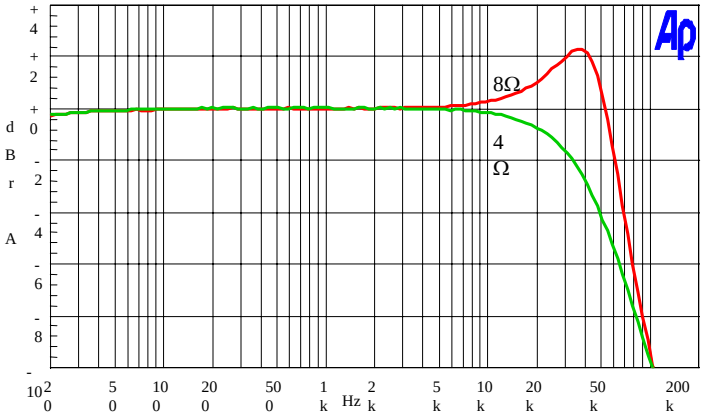
LPF Design Example

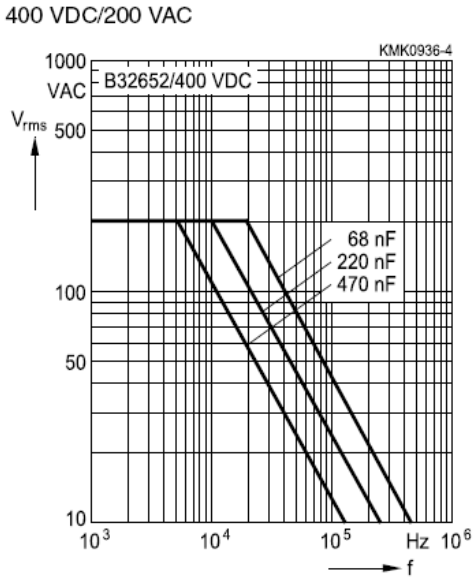
Corner frequency: 40kHz

Load impedance: 4 ohms

Output power: 250W (32Vrms, 11Apeak)







Sagami 7G17B220

22μH, 13A, 10mΩ

Ferrite, closed circuit with inner gap

EPCOS B32652A4474J

Polypropylene, 0.47μF, 400VDC

Chapter 5:
Reducing Noise ~ Noise Isolation Technique ~ PCB Design

Sources of Noise in Class D Amplifier

Switching noise

Switching noise is generated by the output MOSFET switching in wide range of frequency spectrum above the audible range. The amount of switching noise depends on:

- Switching speed
- Size of the MOSFET
- Load current
- PCB layout
- Locations and quality of bypass capacitors

Audio noise

Audio noise is a noise ingredient in audible frequency range in the speaker output. Major causes of audio noise includes:

- Noise figure (NF) in the front-end error amplifier
- Jitter in switching time
- RFI noise from switching noise injection
- Thermal noise from resistors
- Hum noise (AC line 60Hz and its harmonics) from ground loop

Noise Reduction Strategy

1. Minimize noise source in switching stage

2. Maximize noise immunity in analog stage

3. Minimizing noise coupling from switching stage to analog stage

1: Minimizing Noise Source

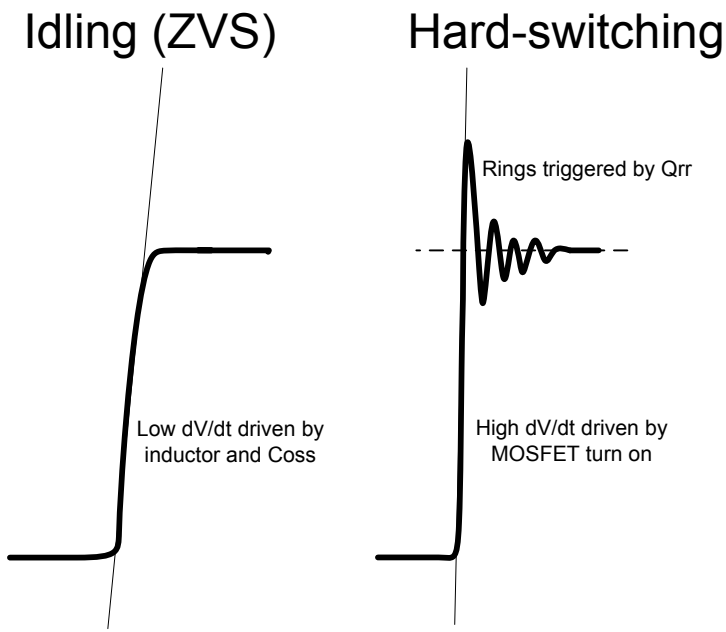
Self-commutation at idling. If rings, check for shoot-through, check dead time.

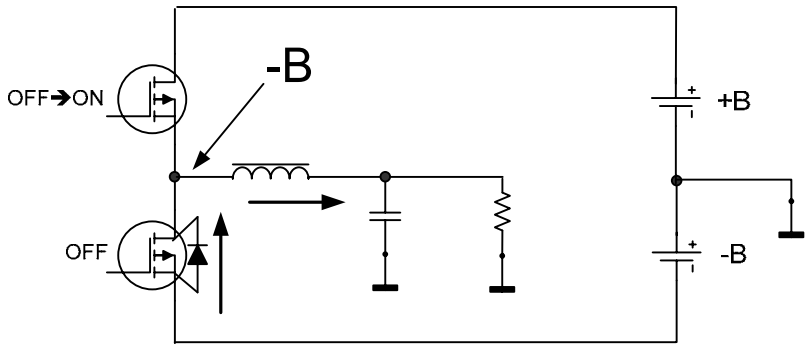
Reverse recovery charge, Qrr, causes hard switching that triggers resonance in stray reactance.

Qrr is a function of di/dt, drain current and die temperature. Slower switching helps to reduce Qrr.

Stray inductance is where excessive energy is stored. Look for optimum trace layouts to minimize stray inductance.

Careful component selection is key to minimize stray reactance.





Reducing Noise with RC Snubber

RC voltage snubber is used to suppress voltage spikes in switching and power supply nodes.

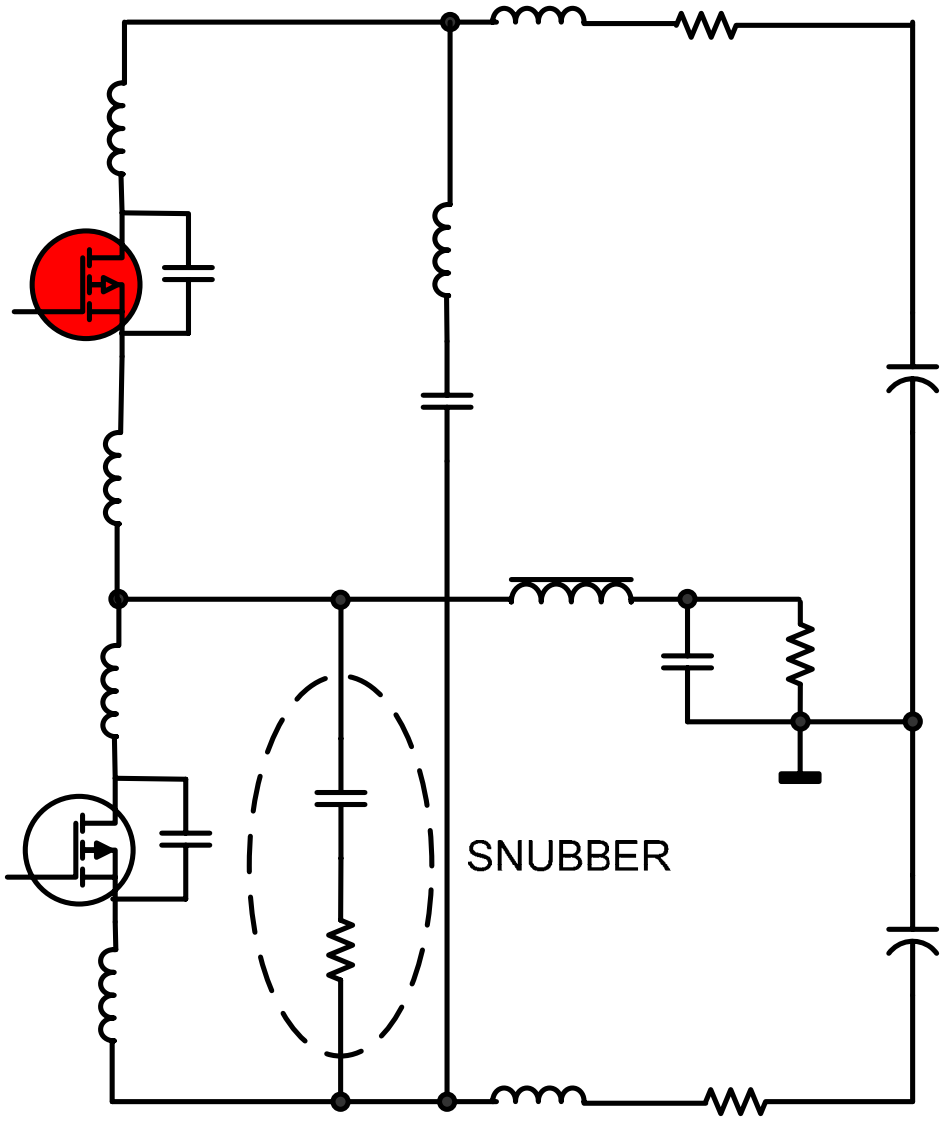
Resistor in RC snubber absorbs energy from reactance by damping resonance.

To maximize effectiveness of a snubber

- Resistance should be close to impedance of resonant element.
- Capacitance should be larger than resonant capacitor.
- Capacitance should be small enough not to cause too much dissipation in the resistor.

Power dissipation from the resistor

$P = 2*f*(\frac{1}{2}CV^2)$



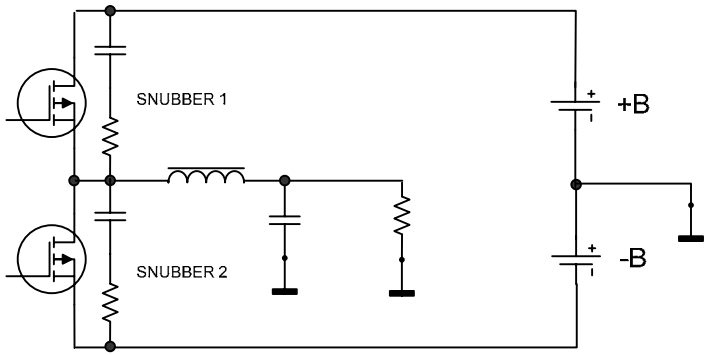
Snubber and THD

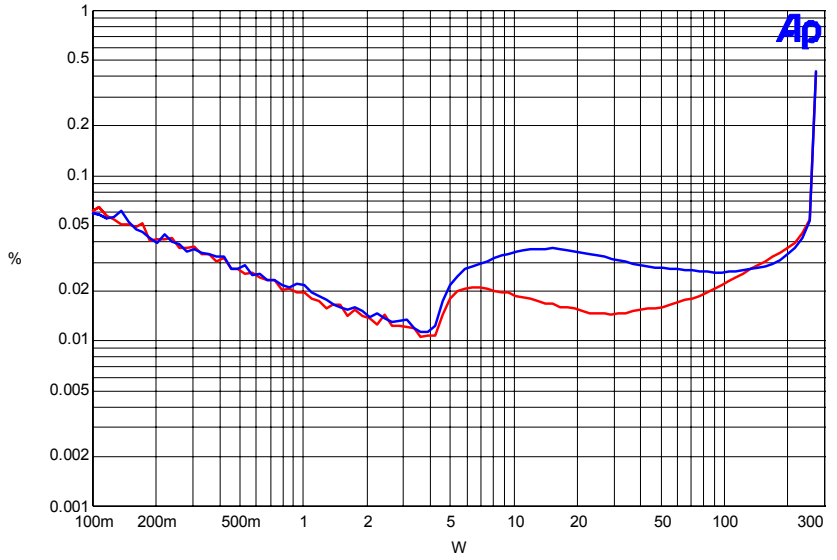
Adding snubber usually improves THD+N.

Change should be in hard switching region.

Basic approach: Make all efforts to minimize stray inductances and current loop areas (minimize resonant energy), then tailor snubber values.

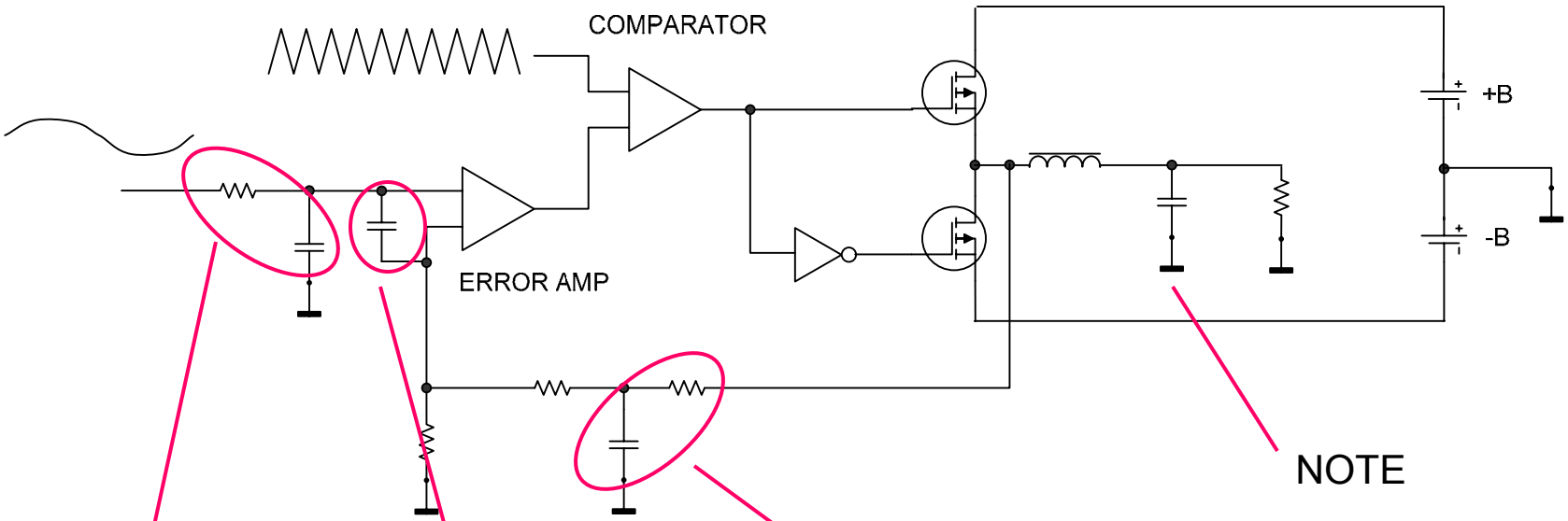
Pay attention to dissipation at snubber.





Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.THD+N Ratio	Left	original+150p+10ohighside
2	1	Blue	Solid	2	Anlr.THD+N Ratio	Left	original (low side snubber onl

2: Maximizing Noise Immunity



Input RF Filter

- Filter out HF noise and reduce node impedance at high frequency

Differential Input RFI Filter

- Prevent RFI causing audio frequency interferences from switching rings

Feedback LPF

- Weed out high frequency spectrum to avoid TIM distortion in the error amplifier

NOTE

- Ground can be a route of noise injection to error amplifier

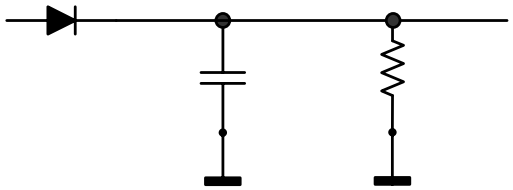
RFI

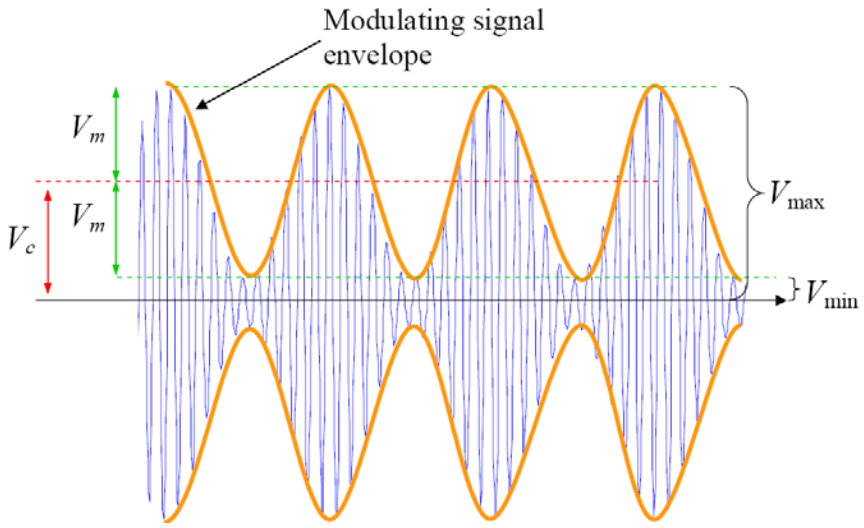
Analog stage uses non-linear components such as diode, BJT and FET.

When a non-linear component receives high frequency components, it detects envelop information that could fall into audio frequency range (amplitude modulation envelop detector).

When non-linear components receives high frequency components along with audio signal, it could shift operating bias point and cause distortion in audio signal.

Diode amplitude detector





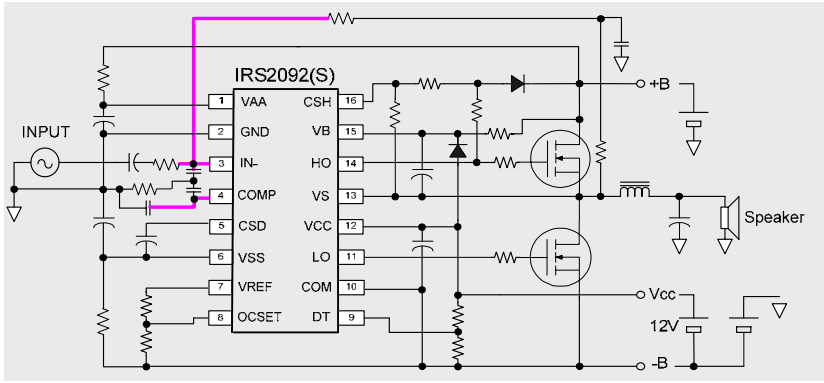
3: Minimizing Noise Coupling

There are functional blocks that generate noise. There are functional blocks that are sensitive to noise. The PCB designer should identify them and find out the best combination of the placement based on these facts and mechanical and thermal requirements.

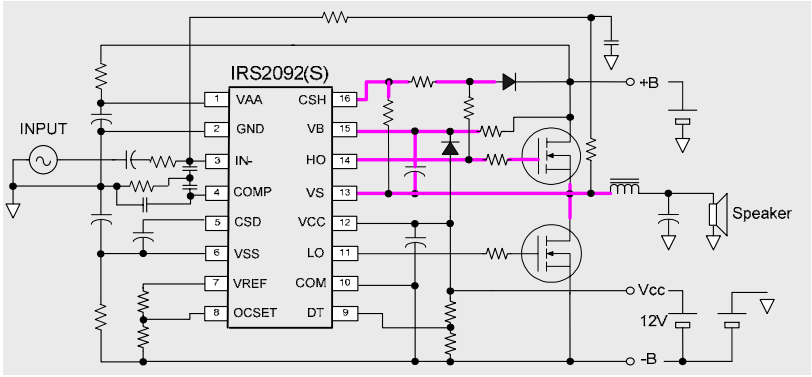
Noise sensitive functions:

- The audio input circuitry
- The PWM control circuitry
- Noise generating functions
- The gate driver stage
- The switching stage

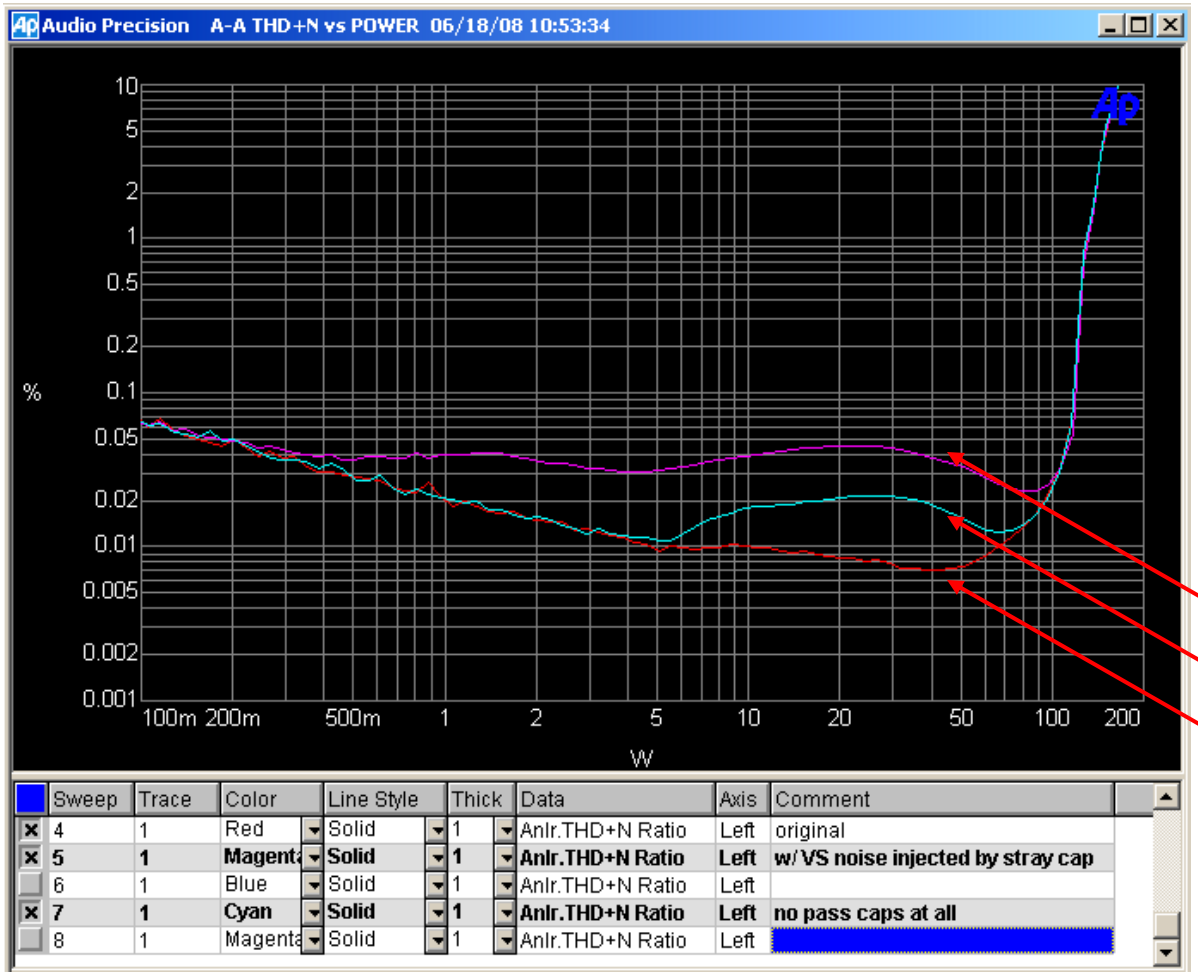
Noise Sensitive Nodes



Noise Generating Nodes



Switching Noise Injection Example



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
4	1	Red	Solid	1	Anlr.THD+N Ratio	Left	original
5	**1**	**Magenta**	**Solid**	**1**	**Anlr.THD+N Ratio**	**Left**	**w/ VS noise injected by stray cap**
6	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	
7	**1**	**Cyan**	**Solid**	**1**	**Anlr.THD+N Ratio**	**Left**	**no pass caps at all**
8	1	Magenta	Solid	1	Anlr.THD+N Ratio	Left	

Noise Coupling from VS

Insufficient Bypass Cap

Original Design (IRAUDAMP7D)

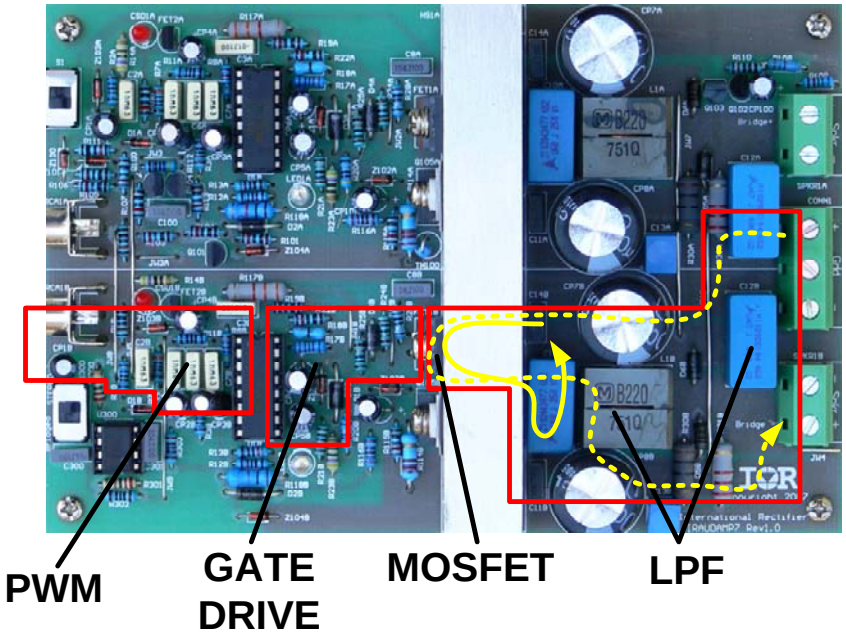
PCB Design Tips

The first and most important step for PCB designers is to group components dedicated to a common purpose, such as:

- the audio input circuitry
- the PWM control circuitry
- the gate driver stage
- the switching stage

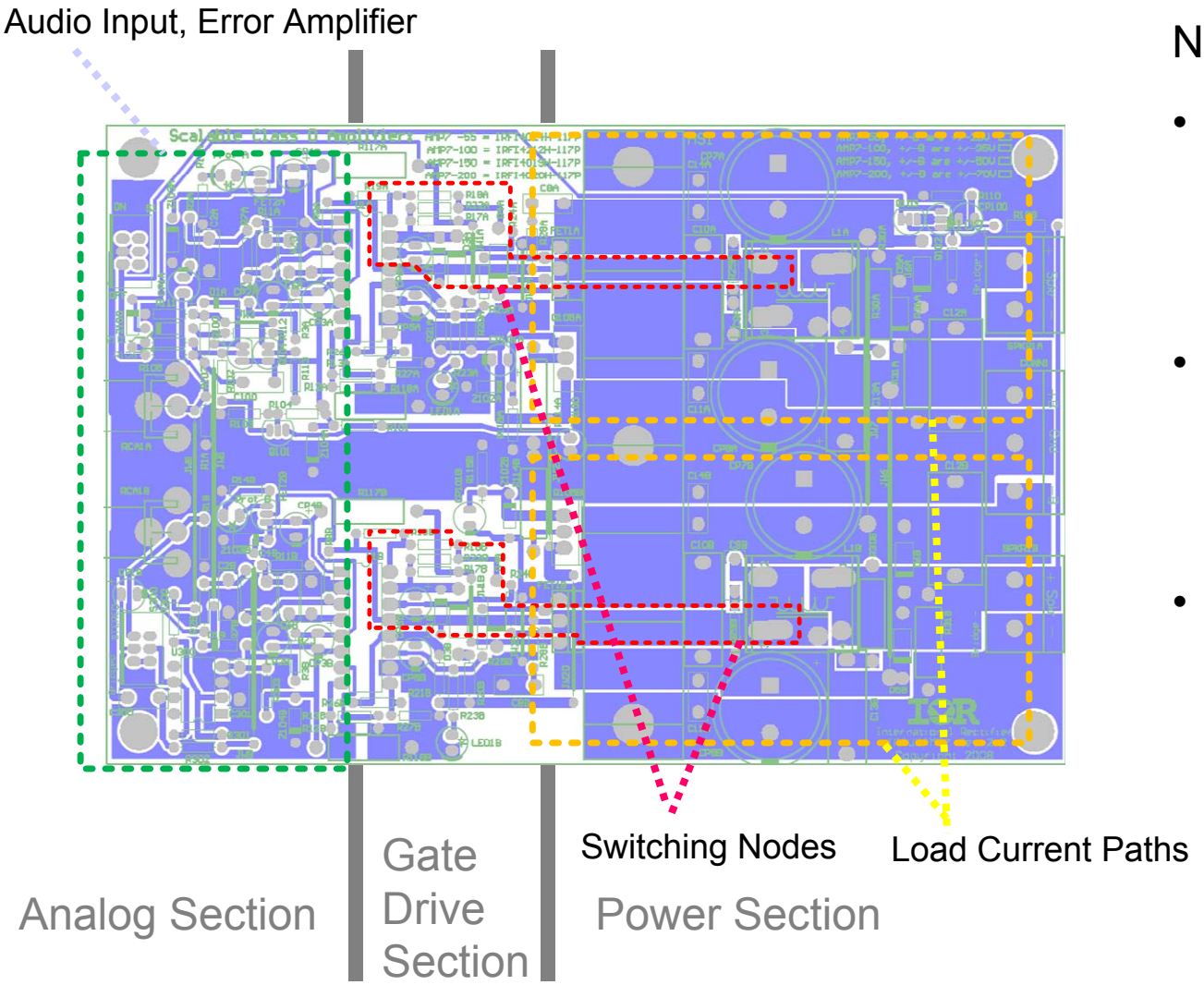
By identifying which components belong together, place the remaining circuitry by coupling them appropriately into open areas of the board.

Key Components Layout Example (IRAUDAMP7D)



Placement Determines Maximum Performance !

PCB Layout Example

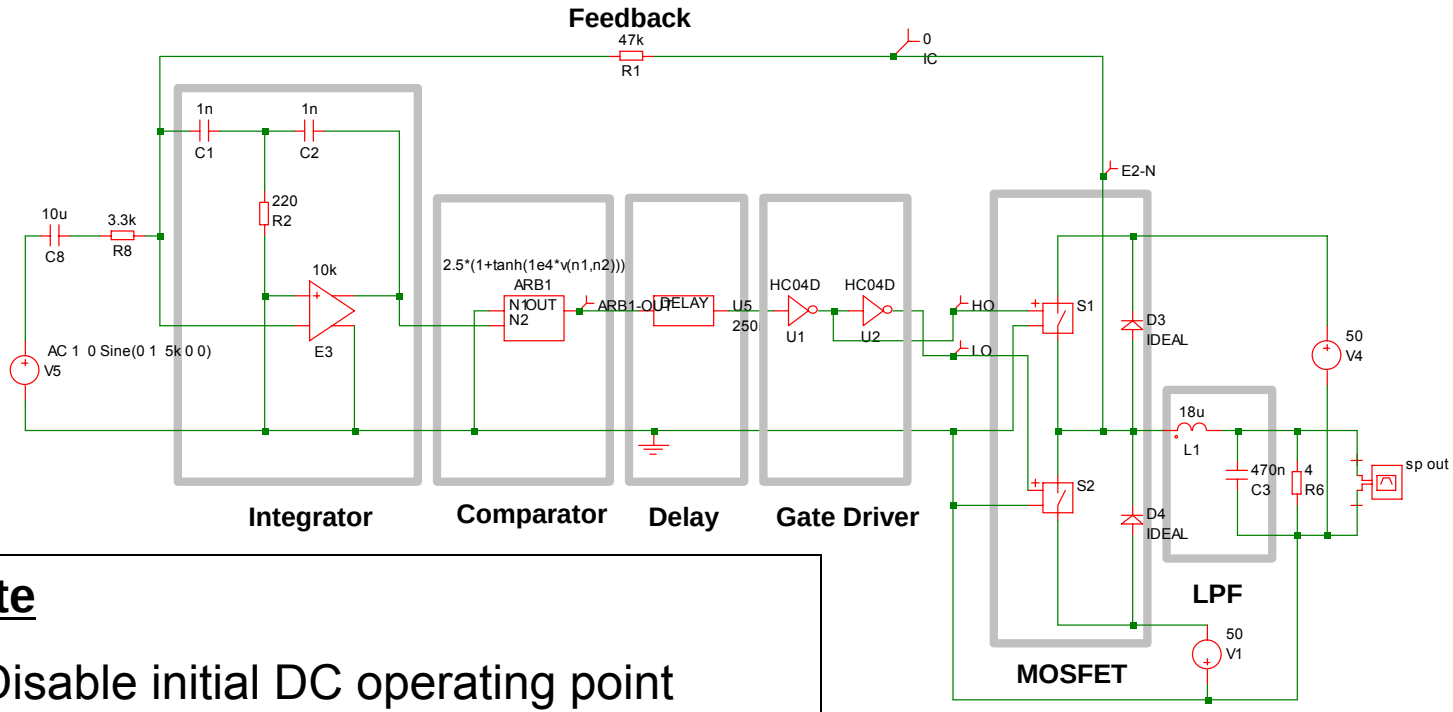


Note that

- Separation between analog and switching sections
- Minimized trace impedances with planes in power section
- No overlap between switching nodes and analog nodes

APPENDIX

Simulation of a Simple Class D Amplifier (SIMetrix)



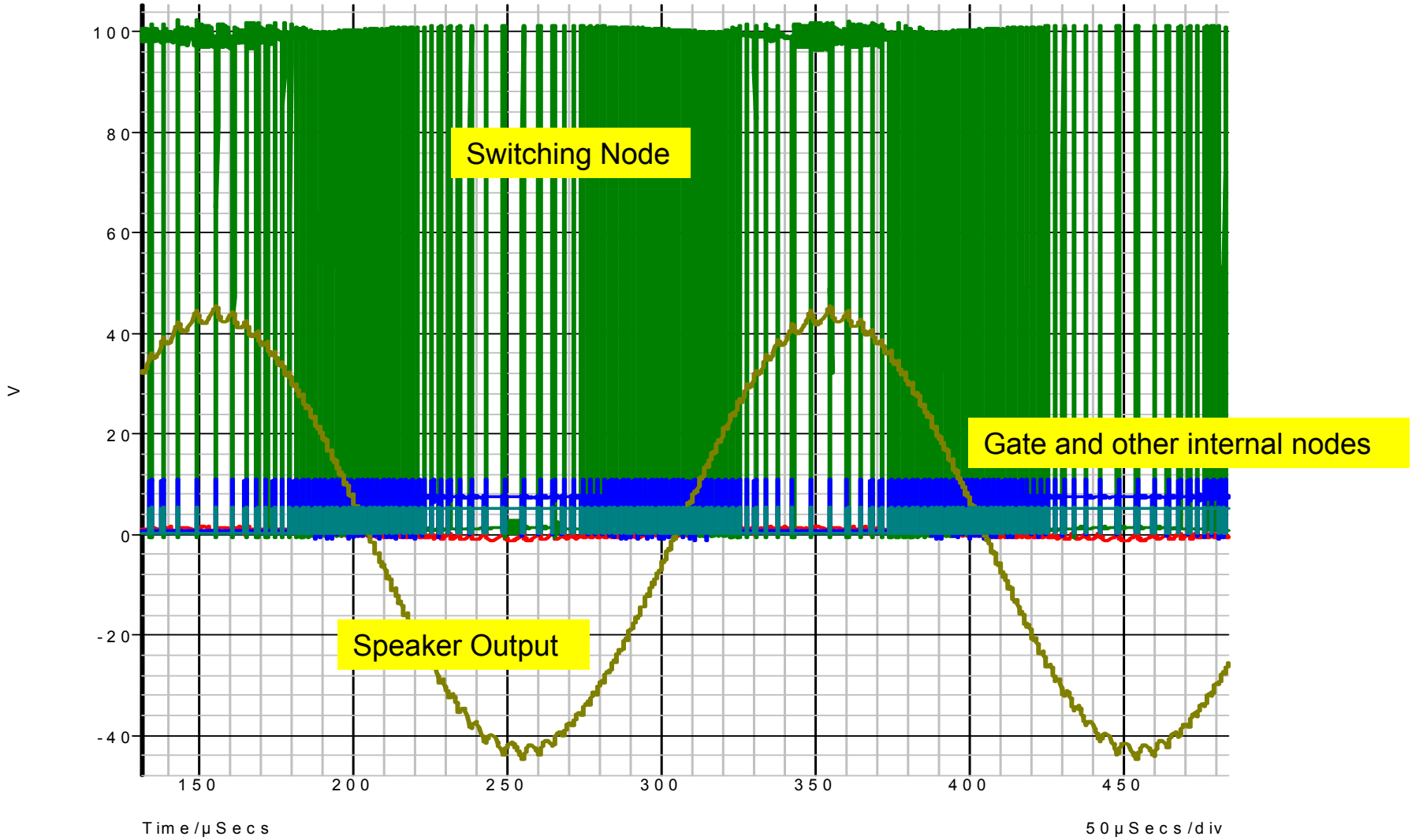
Simulation set up with SIMetrix

Note

- Disable initial DC operating point analysis
- Add initial value in the feedback loop to start off oscillation
- Get into further work once basic ideal model is confirmed

Trial version of SIMetrix can be downloaded from:
http://www.catena.uk.com/

Simulation Result Example



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