Class D Audio Amplifier Design

- **Class D Amplifier Introduction**
  Theory of Class D operation, topology comparison

- **Gate Driver**
  How to drive the gate, key parameters in gate drive stage

- **MOSFET**
  How to choose, tradeoff relationships, loss calculation

- **Package**
  Importance of layout and package, new packaging technology

- **Design Example**
  200W+200W stereo Class D amplifier

Prepared Oct. 8 2003 by Jun Honda and Jorge Cerezo
Trend in Class D Amplifiers

• Make it smaller!
  - higher efficiency
  - smaller package
  - Half Bridge

• Make it sound better!
  - THD improvement
  - fully digitally processed modulator
Class AB amplifier uses linear regulating transistors to modulate output voltage. $\eta = 30\%$ at temp rise test condition.
Class D amplifier uses MOSFETs that are either ON or OFF.

PWM technique is used to express analog audio signals with ON or OFF states in output devices.
Basic PWM Operation

The output signal of comparator goes high when the sine wave is higher than the sawtooth.

Using $f_{PWM}=400\text{KHz}$ to modulate 25KHz sinusoidal waveform
Topology Comparison: Class AB vs Class D

- Gain: Proportional to Vbus
- PSRR: 0 dB
- Direction of energy flow: Both way (Creates Vbus pumping phenomena)
- Efficiency: Constant over Vbus
- Good
- Temp rise test condition

System ➔ Gate Drive ➔ MOSFET ➔ Design Example

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**Analogy to Buck DC-DC Converter**

### Buck Converter

- **Gate Driver**
- **MOSFET (Q1, Q2)**
- **Inductor (L1)**
- **Capacitor (C1)**
- **Load (R1)**

**Load Current Direction**

Duty ratio is fixed
- Independent optimization for HS/LS
- Low $R_{DS(ON)}$ for longer duty, low $Q_g$ for shorter duty

### Class D Amplifier

- **Gate Driver**
- **MOSFET (Q1, Q2)**
- **Inductor (L1)**
- **Capacitor (C1)**
- **Load (R1)**

**Audio signal input as a reference voltage**

Fc of LPF is above 20KHz

Both current directions
- Influence of dead time is different
- Dead time needs to be very tight

Duty varies but average is 50%
- Same optimization for both MOSFETs
- Same $R_{DS(ON)}$ required for both sides

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Loss in Power Device

Loss in class AB

\[ P_c = \frac{1}{2 \cdot \pi} \int_{0}^{\pi} \frac{V_{cc}}{2} (1 - K \sin \omega \cdot t) \cdot \frac{V_{cc}}{2 \cdot R_L} \cdot K \sin \omega \cdot t \cdot d\omega \cdot t \]

\[ = \frac{V_{cc}^2}{8 \pi \cdot R_L} \left( \frac{2K}{\pi} - \frac{K^2}{2} \right) \]

Regardless of output device parameters.

Loss in Class D

\[ P_{TOTAL} = P_{sw} + P_{cond} + P_{gd} \]

\[ P_{cond} = \frac{R_{DS(ON)}}{R_L} \cdot P_o \]

\[ P_{gd} = 2 \cdot Q_g \cdot V_{gs} \cdot f_{PWM} \]

\[ P_{sw} = C_{OSS} \cdot V_{BUS}^2 \cdot f_{PWM} + I_D \cdot V_{DS} \cdot t_f \cdot f_{PWM} \]

K is a ratio of Vbus and output voltage.

Efficiency can be improved further!
## Half Bridge vs Full Bridge

<table>
<thead>
<tr>
<th></th>
<th>Half Bridge</th>
<th>Full Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.5 x 2ch</td>
<td>1</td>
</tr>
<tr>
<td>Current ratings</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>MOSFET</td>
<td>2 MOSFETs/CH</td>
<td>4 MOSFETs/CH</td>
</tr>
<tr>
<td>Gate Driver</td>
<td>1 Gate Driver/CH</td>
<td>2 Gate Drivers/CH</td>
</tr>
<tr>
<td>Linearity</td>
<td>Adjustment is needed</td>
<td>Superior (No even order HD)</td>
</tr>
<tr>
<td>DC Offset</td>
<td>Can be cancelled out</td>
<td></td>
</tr>
<tr>
<td>PWM pattern</td>
<td>2 level</td>
<td>3 level PWM can be implemented</td>
</tr>
<tr>
<td>Notes</td>
<td>Pumping effect</td>
<td>Need a help of feed back</td>
</tr>
</tbody>
</table>

- Suitable for open loop design

![Half Bridge Circuit](image1.png)

![Full Bridge Circuit](image2.png)
Major Cause of Imperfection

- Pulse width error
- Quantization error
- Dead time
- Delay time
- Perturbation
- Zo
- Bus Pumping
- Non linear inductance / Capacitance
- DCR
- Finite $R_{DS(on)}$
- Vth and Qg
- Body diode recovery

ON delay  ->  OFF delay

Finite $dV/dt$
THD and Dead Time

High Side Dead Time

Low Side Dead Time

Dead Time 40nS
THD=2.1%

Dead Time 15nS
THD=0.18%

Note: THD (Total Harmonic Distortion) is a means to measure linearity with sinusoidal signal.

\[
THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots}}{V_{\text{fundamental}}}
\]
Shoot Through and Dead Time

- Shoot through charge increases rapidly as dead time gets shorter.
- Need to consider manufacturing tolerances and temperature characteristics.

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Power Supply Pumping

- Significant at low frequency output
- Significant at low load impedance
- Significant at small bus capacitors
- Largest at duty = 25%, and 75%

Half Bridge

Supply voltage Pumping effect

\[ \Delta V_{BUS}^{\text{max}} = \frac{V_{BUS}}{8 \cdot \pi \cdot f_{PWM} \cdot R_{LOAD} \cdot C_{BUS}} \]

Full Bridge
EMI consideration: Qrr in Body Diode

1. Low side drains inductor current
2. During dead time body diode of low side conducts and keep inductor current flow
3. At the moment high side is turned ON after dead time, the body diode is still conducting to wipe away minority carrier charge stored in the duration of forward conduction.

⇒ This current generates large high frequency current waveform and causes EMI noises.
Gate Driver: Why is it Needed?

- Gate of MOSFET is a capacitor to be charged and discharged. Typical effective capacitance is 2nF.

- High side needs to have a gate voltage referenced to its Source.

- Gate voltage must be 10-15V higher than the drain voltage.

- Need to control HS and LS independently to have dead time.

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**Diagram:**

- HIN
- LIN
- COM
- VCC
- VS
- VB
- VCC
- TO LOAD
- 200V
International Rectifier's family of MOS gate drivers integrate most of the functions required to drive one high side and one low side power MOSFET in a compact package.

With the addition of few components, they provide very fast switching speeds and low power dissipation.
Boot Strap High Side Power Supply

When Vs is pulled down to ground through the low side FET, the bootstrap capacitor ($C_{BOOT}$) charges through the bootstrap diode (Dbs) from the Vcc supply, thus providing a supply to Vbs.

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Boot Strap High Side Power Supply (Cont’d)

- **Boot Strap Capacitor Selection**
  
  \[
  C \geq \frac{2Q_s + \frac{I_{\text{shim}}}{f} + \frac{I_{\text{s}}}{f}}{V_{CC} - V_f - V_{FS} - V_{\text{thr}}}
  \]
  
  where:
  
  - \(V_f\): Forward voltage drop across the bootstrap diode
  - \(I_{\text{thr}}\): Voltage drop across FET (or load for a high side driver)
  - \(V_{FS}\): Minimum voltage between \(V_B\) and \(V_F\)

  To minimize the risk of overcharging and further reduce ripple on the \(V_{BS}\) voltage the \(C_{BS}\) value obtained from the above equation should be multiplied by a factor of 15 (rule of thumb).

- **Boot Strap Diode Selection**
  
  The bootstrap diode (\(D_{BS}\)) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the \(V_{CC}\) supply.

  \[\text{VRRM} = \text{Power rail voltage, } \text{max} \text{ trr} = 100\text{ns, } \text{IF} > Q_{BS} \times f\]

  For more details on boot strap refer to DT98-2

  www.irf.com
Power Dissipation in Gate Driver

Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

\[ P_G = V \cdot f_{SW} \cdot Q_G \]

For two IRF540 HEXFET® MOSFETs operated at 400kHz with \( V_{gs} = 12V \), we have:

\[ P_G = 2 \cdot 12 \cdot 37 \cdot 10^{-9} \cdot 400 \cdot 10^3 = 0.36W \]

For more details on gate driver ICs, refer to AN978.
The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances.

These losses are not temperature dependent.
Layout Considerations

- Stray inductance LD1+LS1 contribute to undershoot of the Vs node beyond the ground.

As with any CMOS device, driving any of parasitic diodes into forward conduction or reverse breakdown may cause parasitic SCR latch up.
Gate Driver for Class D Applications

**IR2011(S)**

**Key Specs**

- $V_{OFFSET}$: 200V max.
- $I_O +/-$: 1.0A /1.0A typ.
- $V_{OUT}$: 10 - 20V
- $t_{on/off}$: 80 & 60 ns typ.
- Delay Matching: 20 ns max.

- Fully operational up to +200V
- Low power dissipation at high switching frequency
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Tolerant to negative transient voltage, dV/dt immune
- SO-8/DIP-8 Package

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How MOSFETs Work

- A MOSFET is a voltage-controlled power switch. A voltage must be applied between Gate and Source terminals to produce a flow of current in the Drain.
MOSFET Technologies (1)

- IR is striving to continuously improve the power MOSFET to enhance the performance, quality and reliability.

- Hexagonal Cell Technology

- Planar Stripe Technology

- Trench Technology
MOSFET Technologies (2)

- Power MOSFET FOMs ($R^*Q_g$) have significantly improved between the released IR MOSFET technologies.
Key Parameters of MOSFETs (1)

- **Voltage Rating, $BV_{DSS}$**

This is the drain-source breakdown voltage (with $V_{GS} = 0$). $BV_{DSS}$ should be greater than or equal to the rated voltage of the device, at the specified leakage current, normally measured at $I_d=250\mu A$.

This parameter is temperature-dependent and frequently $\Delta BV_{DSS}/\Delta T_j (V/°C)$ is specified on datasheets.

$BV_{DSS}$ MOSFET voltages are available from tens to thousand volts.
Key Parameters of MOSFETs (2)

- **Gate Charge, Qg**

This parameter is directly related to the MOSFET speed and is temperature-independent. Lower Qg results in faster switching speeds and consequently lower switching losses.

The total gate charge has two main components: the gate-source charge, Qgs and, the gate-drain charge, Qgd (often called the Miller charge).
Key Parameters of MOSFETs (3)

- **Static Drain-to-Source On-Resistance, $R_{DS(ON)}$**

This is the drain-source resistance, typically specified on data sheet at 25°C with $V_{GS} = 10V$. $R_{DS(ON)}$ parameter is temperature-dependent, and is directly related to the MOSFET conduction losses. Lower $R_{DS(ON)}$ results in lower conduction losses.
Key Parameters of MOSFETs (4)

- Body Diode Reverse Recovery Characteristics, $Q_{rr}$, $t_{rr}$, $I_{rr}$ and S factor.

Power MOSFETs inherently have an integral reverse body-drain diode. This body diode exhibits reverse recovery characteristics. Reverse Recovery Charge $Q_{rr}$, Reverse Recovery Time $t_{rr}$, Reverse Recovery Current $I_{rr}$ and Softness factor ($S = \frac{t_b}{t_a}$), are typically specified on data sheets at 25°C and $\frac{di}{dt} = 100\text{A/us}$.

Reverse recovery characteristics are temperature-dependent and lower $t_{rr}$, $I_{rr}$ and $Q_{rr}$ improves THD, EMI and Efficiency $\eta$.

Typical Voltage –Current Waveforms for a MOSFET Body Diode

www.irf.com
Key Parameters of MOSFETs

- **Package**

  MOSFET devices are available in several packages as SO-8, TO-220, D-Pak, I-Pak, TO-262, DirectFET™, etc.

  The selection of a MOSFET package for a specific application depends on the package characteristics such as dimensions, power dissipation capability, current capability, internal inductance, internal resistance, electrical isolation and mounting process.
Choosing the MOSFET Voltage Rating for Class D applications (1)

- MOSFET voltage rating for a Class D amplifier is determined by:
  - Desired $P_{OUT}$ and load impedance (i.e. 250W on $4\Omega$)
  - Topology (Full Bridge or Half Bridge)
  - Modulation Factor $M$ (80-90%)

$$VB_{DSS\ min} = \sqrt{\frac{2 \times P_{OUT} \times R_{LOAD}}{M}} \times 1.5$$

**Typical additional factor due to stray resistance, power supply fluctuations and MOSFET Turn-Off peak voltage**
Choosing the MOSFET Voltage Rating for Class D Applications (2)

- **Full-Bridge Topology Class D amplifier**

<table>
<thead>
<tr>
<th>Output Power (W)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>25.0</td>
<td>35.3</td>
<td>49.9</td>
<td>61.1</td>
<td>70.6</td>
</tr>
<tr>
<td>150</td>
<td>30.6</td>
<td>43.2</td>
<td>61.1</td>
<td>74.9</td>
<td>86.5</td>
</tr>
<tr>
<td>200</td>
<td>35.3</td>
<td>49.9</td>
<td>70.6</td>
<td>86.5</td>
<td>99.8</td>
</tr>
<tr>
<td>500</td>
<td>55.8</td>
<td>78.9</td>
<td>111.6</td>
<td>136.7</td>
<td>157.8</td>
</tr>
<tr>
<td>1000</td>
<td>78.9</td>
<td>111.6</td>
<td>157.8</td>
<td>193.3</td>
<td>223.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load (Ohms)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30</td>
<td>40</td>
<td>55</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>4</td>
<td>40</td>
<td>55</td>
<td>75</td>
<td>75</td>
<td>100</td>
</tr>
<tr>
<td>6</td>
<td>40</td>
<td>55</td>
<td>75</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>8</td>
<td>75</td>
<td>100</td>
<td>150</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>250</td>
</tr>
</tbody>
</table>

- **Half-Bridge Configuration Class D amplifier**

<table>
<thead>
<tr>
<th>Output Power (W)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>49.9</td>
<td>70.6</td>
<td>99.8</td>
<td>122.3</td>
<td>141.2</td>
</tr>
<tr>
<td>150</td>
<td>61.1</td>
<td>86.5</td>
<td>122.3</td>
<td>149.7</td>
<td>172.9</td>
</tr>
<tr>
<td>200</td>
<td>70.6</td>
<td>99.8</td>
<td>141.2</td>
<td>172.9</td>
<td>199.7</td>
</tr>
<tr>
<td>500</td>
<td>111.6</td>
<td>157.8</td>
<td>223.2</td>
<td>273.4</td>
<td>315.7</td>
</tr>
<tr>
<td>1000</td>
<td>157.8</td>
<td>223.2</td>
<td>315.7</td>
<td>386.6</td>
<td>446.4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load (Ohms)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>55</td>
<td>75</td>
<td>100</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>4</td>
<td>75</td>
<td>100</td>
<td>150</td>
<td>150</td>
<td>200</td>
</tr>
<tr>
<td>6</td>
<td>75</td>
<td>100</td>
<td>150</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>8</td>
<td>150</td>
<td>200</td>
<td>400</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>100</td>
<td>200</td>
<td>250</td>
<td>400</td>
<td>400</td>
<td>450</td>
</tr>
</tbody>
</table>

Note 1. Modulation Factor M = 85%
Calculation of Switching Loss (1)

- Switching Losses are the result of turn-on and turn-off switching times
• Gate resistance $R_g$, and gate charge $Q_g$, have a significant influence on turn-on and turn-off switching times

$\uparrow R_g \Rightarrow \downarrow I_g \Rightarrow \uparrow t_{\text{SWITCHING}} \Rightarrow \uparrow P_{\text{SWITCHING}}$

$\uparrow Q_g \Rightarrow \uparrow t_{\text{SWITCHING}} \Rightarrow \uparrow P_{\text{SWITCHING}}$
Estimation of Switching Losses (1)

- Switching losses can be obtained by calculating the switching energy dissipated in the MOSFET

\[ E_{sw} = \int_{0}^{t} V_{DS}(t) \times I_{D}(t) \, dt \]

Where \( t \) is the length of the switching pulse.

- Switching losses can be obtained by multiplying switching energy with switching frequency.

\[ P_{SWITCHING} = E_{SW} \times F_{SW} \]
Estimation of Conduction Loss (2)

- Conduction losses can be calculated using $R_{DS(ON)}$ @ $T_j$ max and $I_{D\,RMS}$ current of MOSFET

\[ P_{CONDUCTION} = (I_{D\,RMS})^2 \times R_{DS(ON)} \]

$I_{D\,RMS}$ is determined using amplifier specifications:

\[ I_{D\,RMS} = \sqrt{\frac{P_{OUT}}{R_{LOAD}}} \]

$R_{DS(ON)}$ data can be obtained from the MOSFET data sheet.

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Thermal Design

- Maximum allowed power dissipation for a MOSFET mounted on a heat sink:

\[ P_{\text{max}} = \frac{\Delta T_j}{R_{\text{thja max}}} \]

\[ P_{\text{max}} = \frac{(T_{\text{amb}} - T_{j\text{max}})}{(R_{\text{thjc max}} + R_{\text{thcs max}} + R_{\text{ths max}} + R_{\text{thsa max}})} \]

Where:

- \( T_{\text{amb}} \) = Ambient Temperature
- \( T_{j\text{max}} \) = Max. Junction Temperature
- \( R_{\text{thjc max}} \) = Max. Thermal Resistance Junction to Case
- \( R_{\text{thcs max}} \) = Max. Thermal Resistance Case to Heatsink
- \( R_{\text{ths max}} \) = Max. Thermal Resistance of Heatsink
- \( R_{\text{thsa max}} \) = Max. Thermal Resistance Heatsink to Ambient
There is tradeoff between Static Drain-to-Source On-Resistance, $R_{DS(ON)}$ and Gate charge, $Q_g$

- Higher $R_{DS(ON)} \Rightarrow$ Lower $Q_g \Rightarrow$ Higher $P_{\text{CONDUCTION}}$ & Lower $P_{\text{SWITCHING}}$
- Lower $R_{DS(ON)} \Rightarrow$ Higher $Q_g \Rightarrow$ Higher $P_{\text{SWITCHING}}$ & Lower $P_{\text{CONDUCTION}}$
Die Size vs Power Loss (1)

- Die size has a significant influence on MOSFET power losses

Smaller Die ⇒ Higher $P_{\text{CONDUCTION}}$ & Lower $P_{\text{SWITCHING}}$
Bigger Die ⇒ Higher $P_{\text{SWITCHING}}$ & Lower $P_{\text{CONDUCTION}}$
Die Size vs Power Loss (2)

- Die size is directly related with $R_{DS(ON)}$ and $R_{THjc}$ of the MOSFET

  Smaller Die $\Rightarrow$ Higher $R_{DS(ON)}$ and Higher $R_{THjc}$
  Bigger Die $\Rightarrow$ Lower $R_{DS(ON)}$ and Lower $R_{THjc}$
Choosing the Right MOSFET for Class D Applications

- The criteria to select the right MOSFET for a Class D amplifier application are:
  - $V_{B_{DSS}}$ should be selected according to amplifier operating voltage, and it should be large enough to avoid avalanche condition during operation.
  - Efficiency $\eta$ is related to static drain-to-source on-resistance, $R_{DS(ON)}$. Smaller $R_{DS(ON)}$ improves efficiency $\eta$. $R_{DS(ON)}$ is recommended to be smaller than 200m$\Omega$ for mid and high-end power, full-bandwidth amplifiers.
  - Low gate charge, $Q_g$, improves THD and efficiency $\eta$. $Q_g$ is recommended to be smaller than 20nC for mid and high-end power, full-bandwidth amplifiers.
Choosing the Right MOSFET for Class D Application

- Amplifier performance such as THD, EMI and efficiency $\eta$ are also related to MOSFET reverse recovery characteristics. Lower $\text{trr}$, $\text{Irr}$ and $\text{Qrr}$ improves THD, EMI and efficiency $\eta$

- $R_{\text{thjc}}$ should be small enough to dissipate MOSFET power losses and keep $T_J < \text{limit}$

- Better reliability and lower cost are achieved with higher MOSFET $T_{J \text{ max}}$

- Finally, selection of device package determines the dimensions, electrical isolation and mounting process. These factors should be considered in package selection. Because cost, size and amplifier performance depend on it.
Development of Class D Dedicated Devices

- Performance of the Class D amplifying stage strongly depends on the characteristics of MOSFETs and ICs.

- Designers of driver IC and MOSFET silicon need to keep the special requirements of the Class D application in mind.
Influences of Stray Inductance

- PCB layout and the MOSFET internal package inductances contribute to the stray inductance ($L_S$) in the circuit.

- Stray inductances affect the MOSFET performance and EMI of the system.
Influences of Stray Inductance

- Drain and source stray inductances reduces the gate voltage during turn-on resulting in longer switching time.
- Also during turn-off, drain and source stray inductances generate a large voltage drop due to $\text{d}I_D/\text{d}t$, producing drain to source over-voltage transients.

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DirectFET™ Packaging

- Remove wirebonds from package and replace with large area solder contacts
- Reduced package inductance and resistance
- Copper can enables dual sided cooling
DirectFET™ Packaging

- 30A VRM output current
- 500 kHz per phase
- Silicon of the near identical active area, voltage and generation used in both packages
- Inductance related ringing greater in case of SO-8
Class D Amp Reference Design

- **Specs**

  - **Topology:** Half Bridge
  - **IR Devices:** IR2011S, IRFB23N15D
  - **Switching frequency:** 400kHz (Adjustable)
  - **Rated Output Power:** 200W+200W / 4 ohm
  - **THD:** 0.03% @1kHz, Half Power
  - **Frequency Response:** 5Hz to 40kHz (-3dB)
  - **Power Supply:** ~ ±50V
  - **Size:** 4.0” x 5.5”

  [Image of the circuit board]
Class D Amp Reference Board: Block Diagram

- Integrator (LT1220)
- Level Shifter (2N5401)
- Comparator (74HC04)
- Gate Driver (IR2011S)
- Feedback
- MOSFET (IRFB23N15D)
- LPF

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Circuit Diagram

- CH1 Feed Back Path

- Level Shift
- Integrator
- Input analog
- Quantize
- Gate Driver
- Over Current
- LPF
- Speaker output
- Snubber

System ➔ Gate Drive ➔ MOSFET ➔ Design Example
Class D Amp Reference Board: Layout

- Analog Input (CH1)
- Analog Input (CH2)
- Modulator (CH1)
- Modulator (CH2)
- Gate Driver
- MOSFET
- HeatSink
- +5V Regulator
- ±5V
- Power Supply
- Bus Capacitor
- +12V DC/DC
- LPF (CH1)
- LPF (CH2)
- Protection
- Speaker (CH1)
- Speaker (CH2)

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Performance

50W / 4Ω, 1KHz, THD+N=0.0078%

[Graph showing waveform and THD+N vs. Output Power]

342W / 4Ω, 1KHz, THD+N=10%

[Graph showing waveform and THD+N vs. Output Power]

• Peak Output Power (f=1KHz)
  120W / 8Ω / ch, THD=1%
  180W / 8Ω / ch, THD=10%
  245W / 4Ω / ch, THD=1%
  344W / 4Ω / ch, THD=10%

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Performance (Cont’d)

Switching waveform

THD+N v.s. Frequency

Residual Noise: 62.5µVrms, A-Weighted, 30KHz-LPF

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Conclusion

- Highly efficient Class D amplifiers now provide similar performance to conventional Class AB amplifiers - if key components are carefully selected and the layout takes into account the subtle, yet significant impact due to parasitic components.

Constant innovation in semiconductor technologies helps the growing Class D amplifiers usage due to improvements in higher efficiency, increased power density and better audio performance.