

Increasing Efficiency in Secondary-Side Rectification

Replacing Schottky diodes with MOSFETs

Electronic products within a broad range of applications have evolved over recent years, taking advantage of advancing signal- and data-processing silicon technologies to achieve greater functional densities. Significant developments in both IC design and IC fabrication have accelerated this trend.

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An important consequence of these activities is that power supplies now must provide greater currents and, often, in more space-constrained environments than has historically been the case. With growing pressure on power density, supply architecture has become a greater concern in product design.

Some of the greatest power-supply challenges occur in consumer products such as game consoles, PDP and LCD TVs, LCD monitors, laptop computers, home-theatre equipment, and "headless" mini-PCs, which sell under severe price competition and enjoy short model lifetimes. These market constraints combine to severely limit the OEM's design-cycle time while increasing the need for power-supply optimization. As a result, designers must tune their supply designs more tightly or risk a competitor gaining an edge for having done so.

Finally, energy conservation has been growing in importance as a matter of public policy. Legislation such as the EU's EuP (energy-using products) directive 2005/32/EC, specifications such as those from the US EPA EnergyStar program, and the IEA's (International Energy Agency's) 1W-standby initiative serve to highlight the path our industry is on globally.

Synchronous rectification provides greater efficiency and density

Designers turn to synchronous rectification to improve the efficiency of their power-subsystems' secondary-side circuitry. This conceptually-simple modification of a classic topology, such as a flyback converter, can significantly reduce secondary-side dissipation by replacing Schottky diodes with MOSFETs at little or no system-cost penalty. The power level at which such a modification is practical has been decreasing with every new generation of power MOSFETs, so synchronous rectification is applicable to an ever-growing range of products.

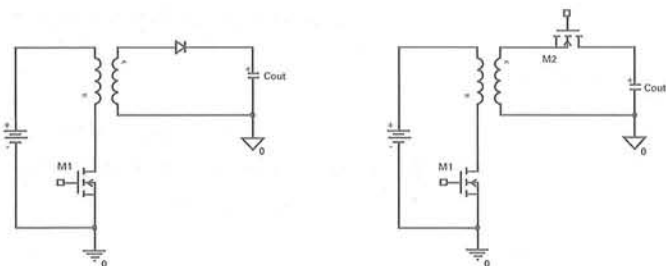


Figure 1: Typical flyback converter and Synchronous Rectifier

For example, a typical flyback converter dissipates between 600 and 720 mW/A in the Schottky diode (Figure 1A). The dissipation follows this linear relation, the slope of which is a function of the device's operating temperature:

$$P_D = V_F(T)I_{DRMS}$$

where P_D is the diode's power dissipation, V_F is the diode's forward voltage at temperature T , and I_D is the diode's forward current. Replacing the diode with a synchronous rectifier (Figure 1) trades the diode's dissipation behaviour for that of the MOSFET. The FET's conduction losses are proportional to the square of the current, but are scaled by the device's channel resistance, which for modern devices is quite small:

$$P_M = R_{DS(on)}(T)I_D^2$$

where P_M is the power dissipation due to the MOSFET's conduction losses, $R_{DS(on)}$ is the MOSFET's channel resistance at temperature T , and I_D is the MOSFET's on-time current. Neglecting, for the moment, additional losses due to the diode's reverse recovery or the MOSFET's switching and body-diode losses, the example of an 18 milliohm MOSFET substantially reduces the secondary-side dissipation (Figure 2).

The MOSFET's smaller dissipation allows designers to take advantage of smaller components with less heat sinking—increasing power density while lowering both BOM and assembly costs, product size, and shipping weight.

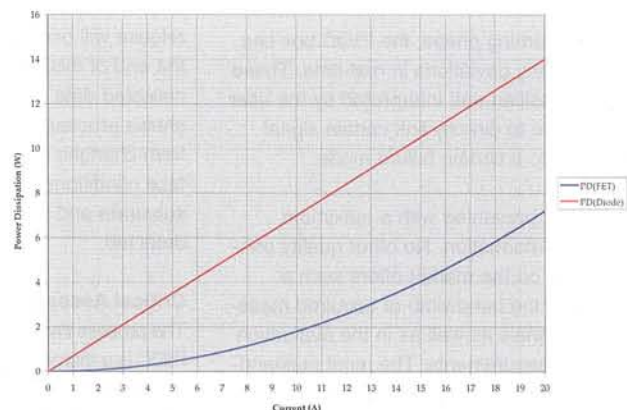


Figure 2: Comparison of MOSFET to Diode Losses

FET-control methods

The challenge to implementing synchronous rectifiers lies in deriving a gate-drive signal with sufficiently precise timing. Imprecise timing quickly degrades the power supply's efficiency by allowing the output-filter components to discharge through the secondary circuit during a fraction of each cycle.

One method of implementing a synchronous rectifier derives the timing from the primary-side waveform. This approach, however, suffers from a number of difficulties. In isolated converters, the timing signal from the primary side to the secondary requires a path across the isolation barrier, which affects significantly, not only the system cost, but also timing synchronization between the two sides of the converter. Timing skew accrues from the differential delay between the power and timing paths. Due to the different mechanisms that implement the two paths, the differential delay is also a function of operating temperature.

The smallest isolation link for a timing signal originating from the primary side is an optocoupler. Though attractive for its size, optocouplers are slow and limit the converter's top operating frequency. This speed limitation affects the size of filter components and impairs the converter's ability to respond quickly to load-current transients.

Circuits that derive their timing from the primary also often perform poorly under light-load conditions. This limitation increases the challenge that energy-conservation programs, such as the 1W-standby initiative, pose.

Of the synchronous-rectifier control methods that derive their timing from the transformer secondary, the best known uses a current transformer to sense the polarity of secondary current (Figure 3). The operation of this circuit is fairly straightforward.

At the beginning of the secondary's conduction phase, the MOSFET is off. When the secondary voltage rises to more than about 0.7V

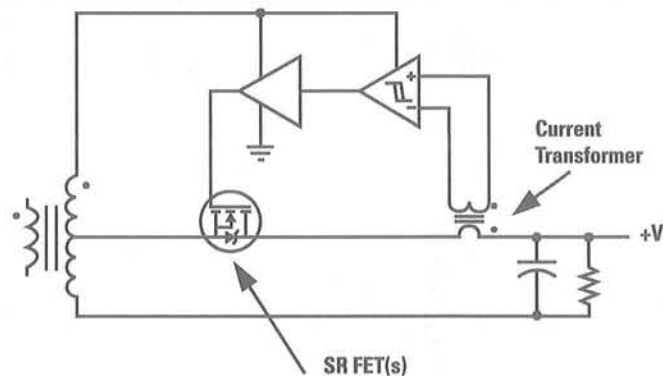


Figure 3: Current transformer to sense the polarity of secondary current

above the filter-capacitor voltage, current begins to conduct through the MOSFET's body diode. A comparator that monitors the secondary through a current transformer detects this positive current flow and changes state, which causes the driver to turn on the FET.

At the end of the conduction phase, the secondary voltage begins to collapse. When the secondary voltage falls below the filter-capacitor voltage, reverse current flows from the capacitor through the MOSFET and the secondary winding to ground. Again, the comparator detects secondary current by way of the current transformer and, owing to the current's polarity reversal, the comparator turns off the gate driver and, by extension, the MOSFET.

This scheme is much more efficient than the Schottky-diode based topology: A typical example of this design for a 120W laptop-computer

er adapter provided an operating efficiency of 87.75% under low-line conditions at 45 degrees C.

But the current-transformer-based design still has its drawbacks. The comparator triggers the MOSFET's off interval after the reverse current has developed to a sufficient amplitude to overcome the polarity-detector circuit's hysteresis. This turn-off delay allows a small percentage of energy stored in the output filter to discharge. The resultant circulating current does nothing but reduce the overall supply efficiency, which adds to the design's thermal load and increases the output ripple for a given charge-storage capacity. The current-transformer sensing method also tends to require many components: The aforementioned 120W laptop-computer adaptor using this approach requires 20 components on the secondary side for the full implementation plus the extra winding on the power transformer.

A smarter rectifier

An alternative method works by directly monitoring the synchronous-rectifier FET. This approach results in faster and more precise timing, requires few parts, and occupies little board space. Indeed, one IC implementation of the method, referred to as the SmartRectifier, reduces the 120W laptop-adaptor example to six parts that fit into an area less than 160 mm².

At the heart of the technique is a provision for switching the synchronous-rectifier FET very near the secondary current's zero crossing (Figure 4).

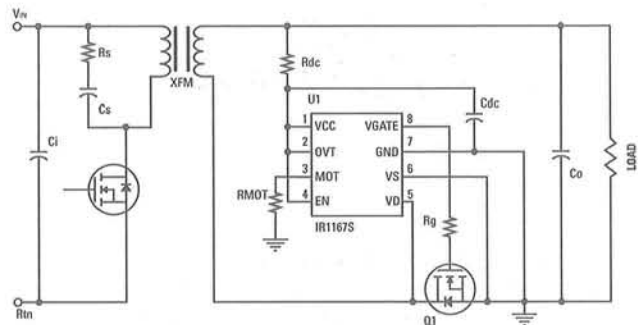


Figure 4: Directly monitoring the synchronous-rectifier FET

To precisely execute the necessary switch timing, a pair of integrated high-speed 200-V comparators sense the FET's drain-source voltage. The comparators operate on three voltage thresholds— V_{TH1} , V_{TH2} , and V_{TH3} —to determine the correct turn-on and turn-off times for the synchronous-rectifier switch (Figure 5).

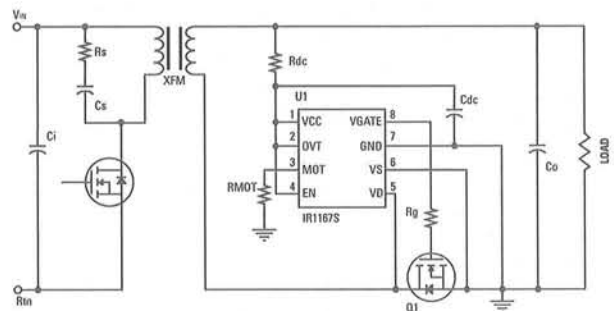


Figure 5: Correct turn-on and turn-off times for the synchronous-rectifier switch

At the start of the secondary's conduction phase, the FET is off and V_{DS} is reversing from positive to negative, presenting a forward bias to the FET's body diode. Current through the body diode forces V_{DS} to exceed V_{TH2} , and the control IC turns on the FET. As the FET turns on, V_{DS} falls to $I_{SEC}R_{DS(on)}$.

For a flyback converter in DCM (discontinuous-conduction mode) or CrCM (critical-conduction mode), the rectified current decreases after the switch turns on. The absolute value of V_{DS} follows the current, decreasing until it reaches V_{TH1} at which point the controller turns off the FET again.

The behaviour under CCM (continuous conduction mode) is slightly different: During the conduction phase the current decays and the drain-source voltage decreases. When the primary-side switch turns back on, the current through the secondary FET rapidly decreases. This forces the drain-source voltage through the V_{TH1} threshold at which point the controller turns off the FET, turning off the FET.

Beyond this basic algorithm, the method requires two additional functions to prevent spurious behaviour. The transient event that accompanies the FET's turn on can excite resonances in the secondary circuit, which can briefly drive V_{DS} below V_{TH1} . To prevent the controller from misinterpreting this threshold crossing as a normal end of cycle, implementations of this method impose a minimum on time. This feature imposes a minimum duty cycle on the secondary circuit and a

corresponding maximum duty cycle on the primary-side switch.

A similar precaution is necessary at the end of the conduction phase: When the FET turns off a small residual secondary current continues to flow through the FET's body diode, causing V_{DS} to snap past V_{TH2} on the gate drive's falling edge. To prevent the controller from misinterpreting this event as the start of a conduction cycle, a blanking period begins with the gate drive's falling edge. During this interval, the controller does not respond to the V_{TH2} threshold crossing. The blanking period ends when V_{DS} crosses V_{TH3} at which point the device resumes its basic operation.

This synchronous-rectifier-control method reduces switching losses by briefly allowing current flow through the body diode before turning on the switch, imposing conditions on the FET very similar to ZVS (zero-voltage switching). The effect is to reduce the gate-charge that the gate driver must supply to the FET.

In addition to producing converter's losses on the order of 8% less than the current-transformer method, this alternative also reduces the converter's parts count by 75% and, as a consequence, reduces PCB area, BOM and assembly costs.

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