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Lead-free Packaging for Discrete Power Semiconductors

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Introduction

For many decades the electronics industry was well served by solders incorporating lead, Pb. The tin/lead, SnPb, eutectic solder has been the industry standard material for attaching various components to PCBs. This is all about to change as consumer and legislative pressure increases the demand for environmental initiatives within the electronics industry. One of these initiatives is the replacement of Pb-bearing solders with Pb-free solders, perceived to be more environmentally friendly. The removal of Pb from solder has been accelerated by legislation. In Europe, legislation has been drafted in the form of the WEEE/ROHS (Waste Electronic and Electrical Equipment / Restriction of Hazardous Substances) legislation. Under this legislation, Pb will be banned from electrical and electronic equipment by 1st January 2006. Landfill laws within Japan, making Pb-containing electronic waste more expensive to dispose; have also hastened the introduction of Pb-free solders.

The Japanese consumer electronics manufacturing companies seem to be leading the way in the introduction of Pb-free products. The well-documented release and success of the Pb-free Panasonic Minidisc player has highlighted the market advantage that "environmentally-friendly" products can create. Panasonic, Sony, Fujitsu, NEC and others have company policy committed to abolishing Pb-containing solders – some as early as CY2002[1]. More and more companies are now releasing lead-free consumer products, even though the EC deadline is still a few years away.

The considered replacements for the SnPb eutectic solder are mainly Sn solders with additions of various other metals such as; silver, copper, bismuth, antimony, indium etc. The majority of these solders have a higher solidus temperature than the Sn/Pb eutectic whose solidus temperature is 183°C. This naturally drives up the temperatures of manufacturing operations such as reflowing components to PCBs. The most likely replacement to the Sn/Pb eutectic for board attach applications is the tin/3.8silver/0.5copper, SAC, solder whose solidus temperature is 217C, over 30°C higher than the Sn/Pb eutectic. The SAC solder has been recommended by a number of industry bodies[2,3]. This means reflow temperatures may have to rise by a similar temperature, to peak temperatures approaching 260°C.

The technical challenges for component manufacturers can be split into two separate categories. Firstly, there is the replacement of lead-containing materials to a Pb-free alternative. Secondly, there is the re-qualification, and in some cases redesign of packages to ensure reliability through higher processing temperatures. This temperature rise during reflow poses the greatest technical problem to component manufacturers, as most current packages have only been designed to withstand Sn/Pb processing, with peak reflow temperatures of between 225-235°C. This paper discusses some of these problems with specific relation to power semiconductor packages.

Replacing the Lead in Power Semiconductors

Pb can be found in two places in power semiconductor packages. It can be used in high-Pb solders, often used for die attach, it is also used as a termination finish on leads to aid solderability of components.

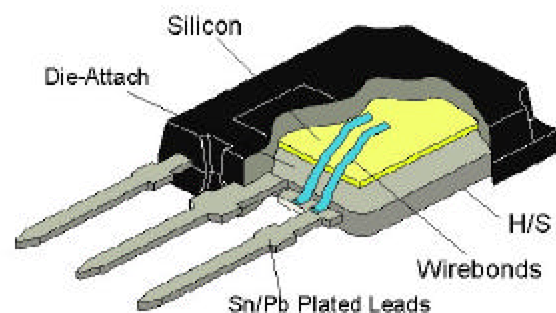


Figure 1: Typical construction of a power semiconductor

Die-attach: High-Pb solders have been used for die-attach applications for many years within the power sector. These solders offer acceptable cost, processibility and performance. Many small power packages already use a lead-free die-attach in the form of Ag-filled epoxy resins. Ag-filled epoxies are low-cost and offer good resistance to reflow temperatures. They are loaded with up to 70% silver

– hence show conductivity suitable for die-attach application. Their use, however, has not yet been expanded to larger silicon sizes in larger power packages. Ag-filled epoxies have been tested by temperature cycling on larger components such as TO220. These experimental components were temperature cycled between –40C and 125C. The samples were monitored using a ? Vsd measurement test. In this test the power dissipation through the package is measured using the temperature sensitive voltage drop across the body drain diode of a power HEXFET™. High magnitudes of ? Vsd indicate high transient thermal impedance – which can be a marker for die-attach degradation during temperature cycling. These experiments included a control vehicle using a standard high-Pb die-attach solder. A comparison of results (figure 2) show that the performance of the Ag-filled epoxy degrades consistently through the temperature cycling, where as the lead based solder remains relatively constant throughout. This shows the unsuitability of Ag-filled epoxy resins for die-attach applications with large silicon where thermal conductivity and electrical resistance are critical.

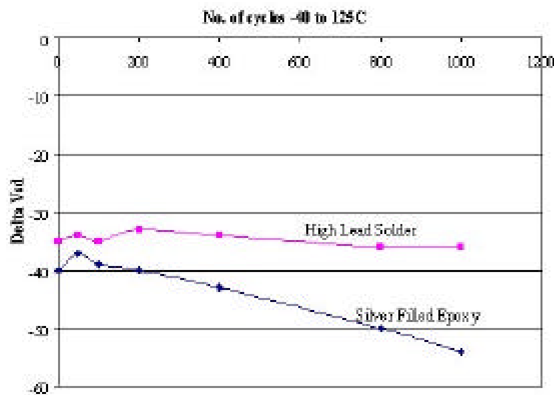


Figure 2: Delta Vsd change through temperature cycling using Ag-filled epoxy as die-attach

The metallurgical options for replacing Pb-based solders for die attach are few. Pb-free alloys are currently used for die-attach application in the form of SnAgSb type solders. These solders perform well in a large number of current applications. In many cases SnAgSb type solders offer better thermal cycling properties than Pb-based die-attach solders. Unfortunately they tend to have low solidus temperatures; typical solidus temperatures are around 225-235°C, followed by a large pasty range. This means that with the increased reflow temperature associated with lead-free board-attach processes, SnAgSb solders will partially melt during soldering. This partial melting can induce voids and cracks into the die-attach layer – reducing thermal impedance and electrical conductivity of the package. This suggests that die-attach solders need to exhibit a solidus temperature above the peak temperatures of the reflow profiles used for board-attach. It has been widely accepted that at present there are no Pb-free metallurgical solutions for die-attach application, this is reflected in an exemption listed in the latest EU legislation for high-Pb type solders[4]. Figure 3 shows some recognised metallurgical die-attach solders, it can be seen that the solders with solidus temperatures above 260°C are all Pb-based.

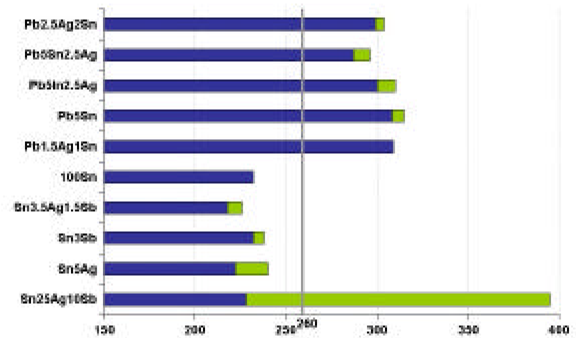


Figure 3: Die-attach solders with solid temperature range( ), and pasty range( )

Termination finish: Historically, leads of power semiconductor packages have been plated with a 90Sn10Pb finish to aid solderability. The obvious replacement is pure tin. Pure tin offers excellent solderability and wetting at a low cost. Also, the fact that it is a single metal alloy increases the desirability from a manufacturing viewpoint. Some plating solutions containing more than one metal can create problems regarding compositional drift.

The one downside for the pure tin plating solution is the relatively poorly understood “tin whisker” phenomenon. Tin whiskers are single crystals of pure tin, thought to be a result of internal stresses within the plating layer. There has been much research to identify the causes of whiskers, but no definitive answer of how to unambiguously stop whisker formation has yet been found. It has been suggested recently that a number of steps can be taken to reduce the likelihood of whisker formation. These steps are[5]:

i) Use a large grain size.
ii) Use a nickel underlayer if the substrate contains copper.
iii) Use a thick plating layer.
iv) Monitor compressive stress build up.

It has also been suggested that the reflow process can act as a whisker suppressant by relieving the stresses within the plating. This may suggest that whisker formation is more of a storage issue than a reliability issue.

A series of experiments has been set up to investigate tin whisker growth on plated power semiconductor devices. Some of this work is presented here. A number of different plating solutions from different manufacturers are being investigated. The samples have been placed in an oven at 55°C (the accepted temperature most likely to promote whisker growth) and are inspected on a regular basis using optical and scanning electron microscopy. 55°C is also a typical temperature of a power semiconductors leads when the component is in use. In the 15 months of inspection to date, we have found that some solutions exhibit whisker growth and some solutions are whisker free. The worst case of whisker growth in these trials exhibited a small number of whiskers with a maximum length of 25 ?m and a diameter of 10 ?m (see figure 4). The whisker growth patterns in these experiments showed no relationship to whether or not the component leads had been formed or not.

The best cases showed no whisker growth after 15 months inspection. These trials are still ongoing.

Figure 4. Example of a tin whisker grown on a pure tin plated surface

Other suggested ways of reducing the risk of whiskers include using a Sn alloy with a small percentage, between 0 and 3 percent, of another metal. Suggested alloys include SnBi, SnCu, and SnAg. These binary alloys are thought to act as whisker suppressants. There are however separate issues with these alloys. Naturally the plating chemistry will be slightly more expensive, but more importantly the process control will be reduced from the primary pure tin plating solution. SnBi is notoriously difficult to control and can require frequent machine maintenance due to the "sludge" produced during process. The other concern regarding the SnBi alloy is the compatibility with any lead containing solders due to the low melting phase produced between Bi and Pb.

In summary, the best solution to replace the SnPb solder plate is a pure tin solution. This offers the best manufacturability and solderability/ wetting characteristics at the best cost.

Temperature Resistance of SMD Components

Aside from material changes, the broad implementation of lead-free solders will ultimately mean higher processing temperatures through the reflow operation. These increased temperatures undoubtedly raise reliability concerns with regards to power components. The increased temperatures themselves do not necessarily cause immediate failure. Instead, the package integrity can be damaged to such an extent that the long-term reliability of the component is negatively affected. Power components are subjected to a rigorous qualification procedure prior to qualified product release. The standard tests for SMD components include:

i) Preconditioning: consisting of temperature and humidity soak followed by reflow (eg 168Hrs @ 85°C/85% RH followed by 3 x reflow @ peak temp of 260°C).
ii) Thermal cycling.
iii) Power cycling.
iv) Temperature humidity bias, THB: 1000hrs @ 85°C/85% RH.
v) Autoclave, A/C: 96Hrs @ 121°C/85% RH/2 atm.

Tests ii, iii, iv and v are carried out after the components have gone through preconditioning. The level of preconditioning given to components ultimately decides the MSL (moisture sensitivity level) of the package. MSL level 1 represents the most extreme levels of preconditioning, and hence the best resistance to moisture and other atmospheric conditions. If a package cannot attain MSL level 1, then it is downgraded to MSL level 2 or less. Packages assigned these lower MSL levels are required to be dry-packed, which is highly undesirable from a manufacturing point of view. The increased temperatures of lead-free reflow profiles could lead to reduction in the MSL level of power components.

Loss of package integrity, in the form of mold compound delamination during reflow can leave a component susceptible to moisture related failures during tests such as THB and autoclave. Mold compound delamination is mainly caused by a coefficient of thermal expansion, CTE, mismatch between the mold compound and the heatsink and silicon. Figure 5 shows the relative CTE values of the main constituents of a power component. The mold compound has two values, alpha 1 and alpha 2.

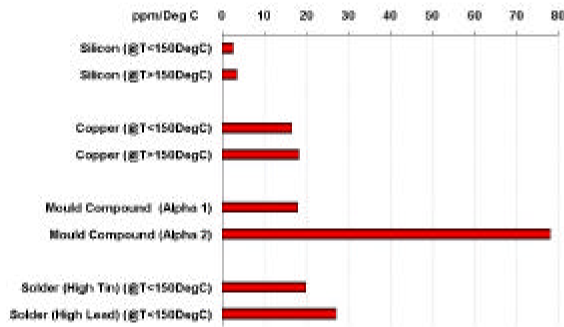


Figure 5. Typical CTE values of semiconductor materials

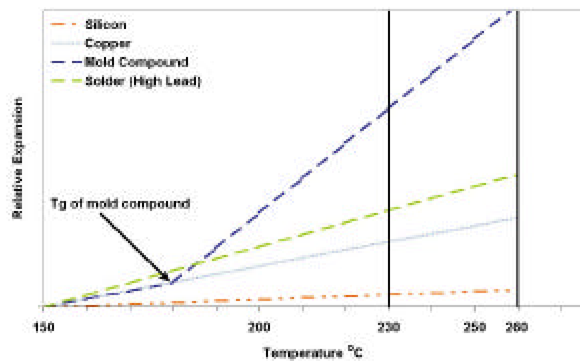


Figure 6. Relative rates of expansion for semiconductor materials

These represent the CTE values below and above the glass transition temperature, Tg, of the mold compound respectively. Typical mold compound Tg temperatures are in the range of 160-190°C. Figure 6 represents the thermal mismatch between mold compound and the other constituents at 230°C and 260°C. It can be seen from this diagram how the increase of 30-40°C required by a lead-free reflow can significantly increase this thermal mismatch – increasing the likelihood of mold compound delamination. This delamination between the mold compound and the leadframe can lead to moisture related failures. Delamination is also caused by the rapid vaporisation of moisture present in the package after the preconditioning soak. This is sometimes known as the "popcorn effect". In the most extreme cases, the popcorn effect can lead to cracks in the component encapsulation.

Figure 7 shows CSAM (C-Scanning Acoustic Microscopy) images of a surface mount package before reflow, after reflow with a 230°C peak and after reflow with a 260°C peak. It can be seen that after 230°C reflow, there is no delamination between the mold compound and the copper heat sink or the silicon die. However, after 260°C reflow, there is delamination present both between the mold compound and heatsink, and the mold compound and die. This doesn't mean certain failure but the delamination could open up path for external moisture to reach the silicon.

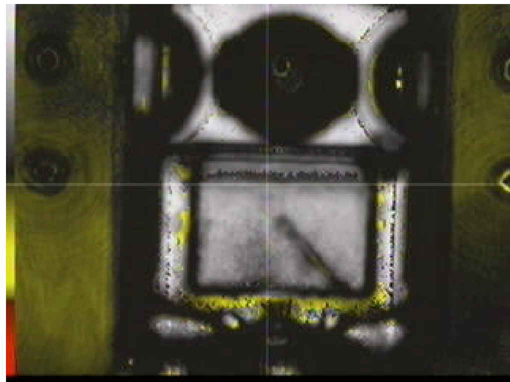
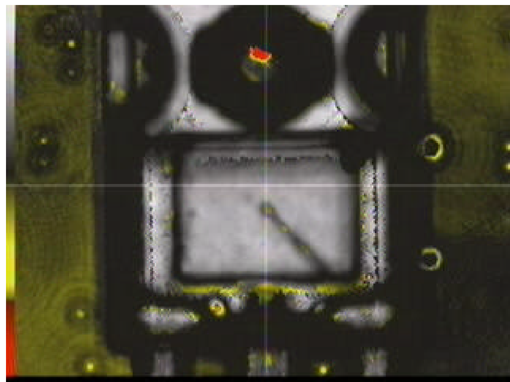
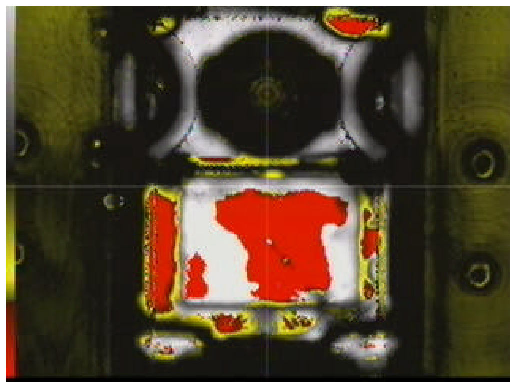


Figure 7. SMD package a) before reflow. (Red areas show delamination)



b) after 230°C reflow



c) after 260°C reflow

Moisture related failures tend to be caused by corrosion to the silicon top metal or bond wires. The path the moisture takes to reach the silicon is along the interface of mold compound and heatsink / leadframe.

There are a number of design aids used by engineers to increase the packages resistance to moisture ingression of this type. Mold locks can increase both the adhesion of the mold compound to the heatsink, and increase the distance external moisture has to

travel to reach the silicon. Examples of the types of mold locks can be seen in figure 8.

The increased reflow temperatures associated with lead-free reflow processes may require some packages to have additional or modified mold locks to achieve qualification. However, introducing new leadframes is expensive and undesirable from a manufacturing viewpoint, so is seen as a last resort.

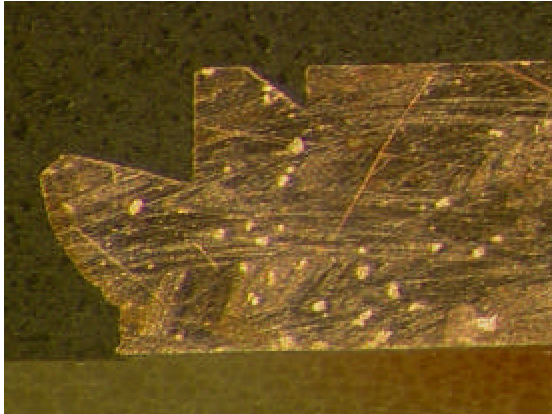
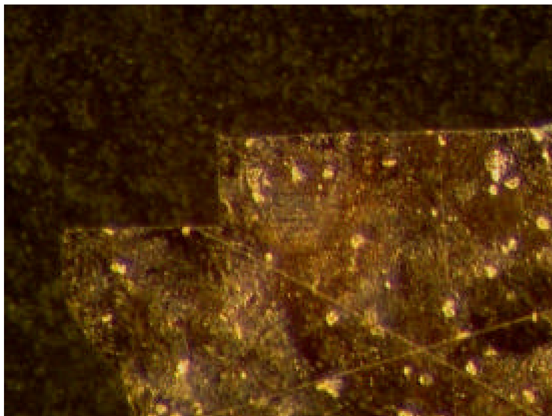


Figure 8a: Examples of mold locks on copper leadframes



b) see figure 8a

Summary

Preparing discrete power semiconductors for lead-free reflow processes raises many technical challenges. There are suitable solutions for replacing Pb in the termination finish, but options for replacing the die-attach solder are few, especially for larger silicon sizes. From a legislative viewpoint, Pb-containing die-attach solutions will be exempt from the WEEE/ROHS legislation.

The greater technical challenge is the upgrade of some existing packages to the elevated reflow temperatures associated with Pb-free manufacturing. Although many packages will not need major modification, undoubtedly there are a number that will need significant change of materials, package redesign or process modification.

References

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2 "NEMI Group Recommends Tin/Silver/Copper as Industry Standard for Lead-free Solder Reflow in Board Assemblies", http://www.nemi.org/PbFreePUBLIC/index.html

3 "Lead-Free: The Way Forward", http://www.lead-free.org/download/files/pdf/lead_free_thewayforward.pdf

4 Amended proposal for "The Restriction on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment" *Brussels, 06.06.2001*

5 "Understanding Whisker Phenomenon – Driving Force for the Whisker Formation" Xu, C; Zhang, Y; Fan, C; Abys, J; Hopkins, L; Stevie, F. *Presented at IPC SMEMA Council APEX 2002.*