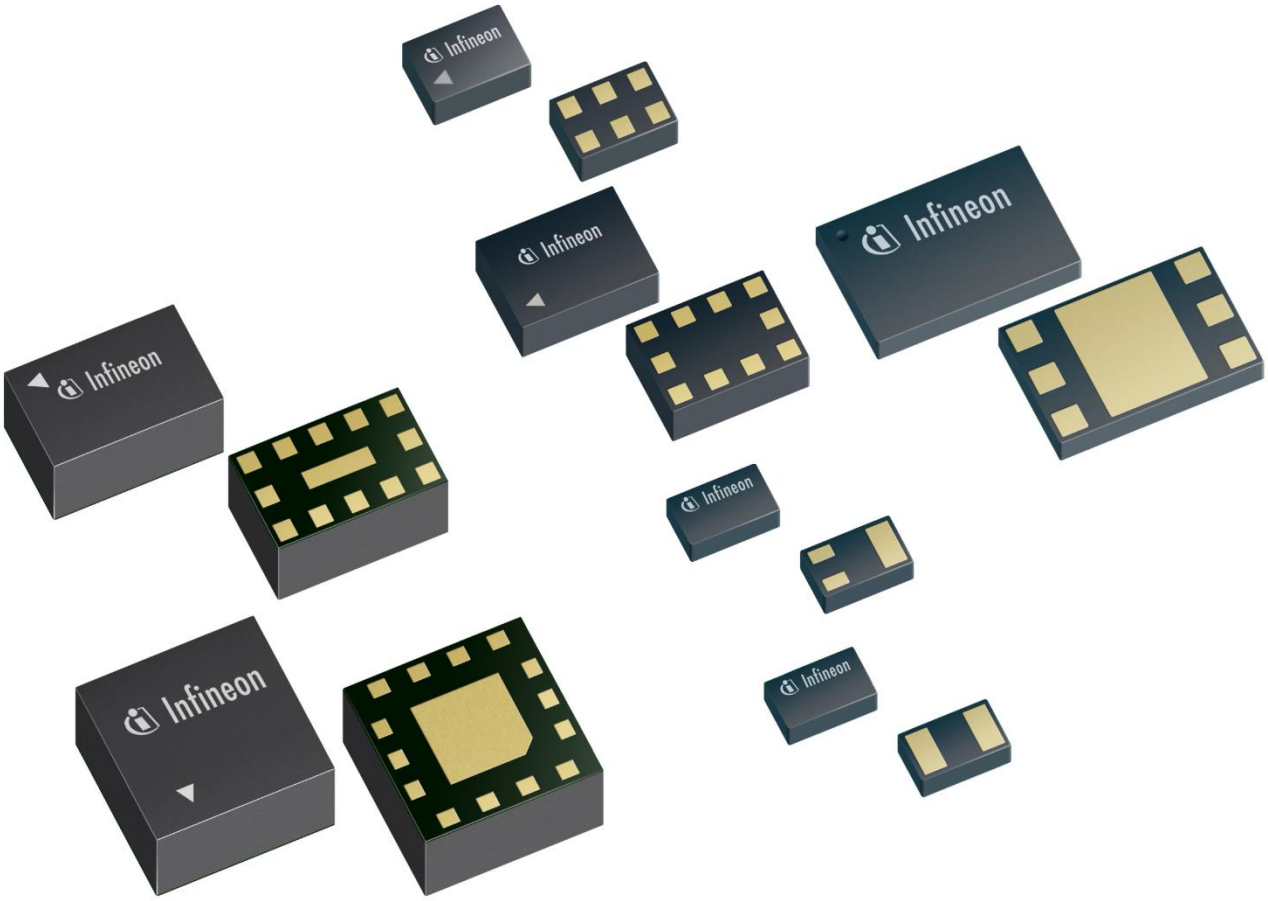
Recommendations for Board Assembly of Infineon Packages with Land Grid Array Configuration



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
ATSLP	Advanced Thin Small Leadless Package
AXI	Automated X-ray Inspection
ESD	Electrostatic Discharge
I/O	Input/Output
LGA	Land Grid Array
MSL	Moisture-Sensitivity Level
Ni/Au	Nickel/Gold
NSMD	Non-Solder Mask Defined pad
PG	Plastic Green
PCB	Printed Circuit Board
RDL	Redistribution Layer
RF	Radio Frequency
SAC	Tin Silver Copper (SnAgCu)
SG	Silicon Green
SMD	Solder Mask Defined
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
SPI	Solder Paste Inspection
TFLGA	Thin Fine pitch Land Grid Array
TSLP	Thin Small Leadless Package
TSNP	Thin Small Non-leaded Package
TSSLP	Thin Super Small Leadless Package
ULGA	Ultra-thin profile Land Grid Array
WLL	Wafer-Level Leadless package

1 Package Description

This document provides information about the Surface Mount Technology (SMT) board assembly of Infineon Thin Small Leadless Packages (TSLP) and Land Grid Array packages (LGA) having bottom-only terminations. Their small size allow for lowest insertion losses making them ideal for carrying devices such as Radio Frequency (RF) switches or low noise amplifiers. They are also capable of carrying multiple dies. They are preferred packages for space- and weight-limited applications such as cellular phones and digital cameras.

This document does not discuss Wafer Level Leadless packages (WLL) or Thin Small Non leaded Packages (TSNP) although there can be identical footprints (e.g. PG-TSSLP-2-1 vs. SG-WLL-2-1 or PG TSLP-16-1 vs. PG-TSNP-16-1). These package families are described in separate documents.

1.1 T(S)SLP Package Type

Infineon TSLP feature a thickness of below one millimeter while Thin Super Small Leadless Packages (TSSLP) can reach a thickness of below half a millimeter. The T(S)SLP familes are partially assembled on a copper carrier but feature no classical leadframe. The T(S)SLP have 2 pins only. **Figure 1** shows examples of the T(S)SLP package families.

- PG-TSLP packages
- PG-TSSLP packages

PG = Plastic Green
T = Thin
S = Super
SLP = Small Leadless Package

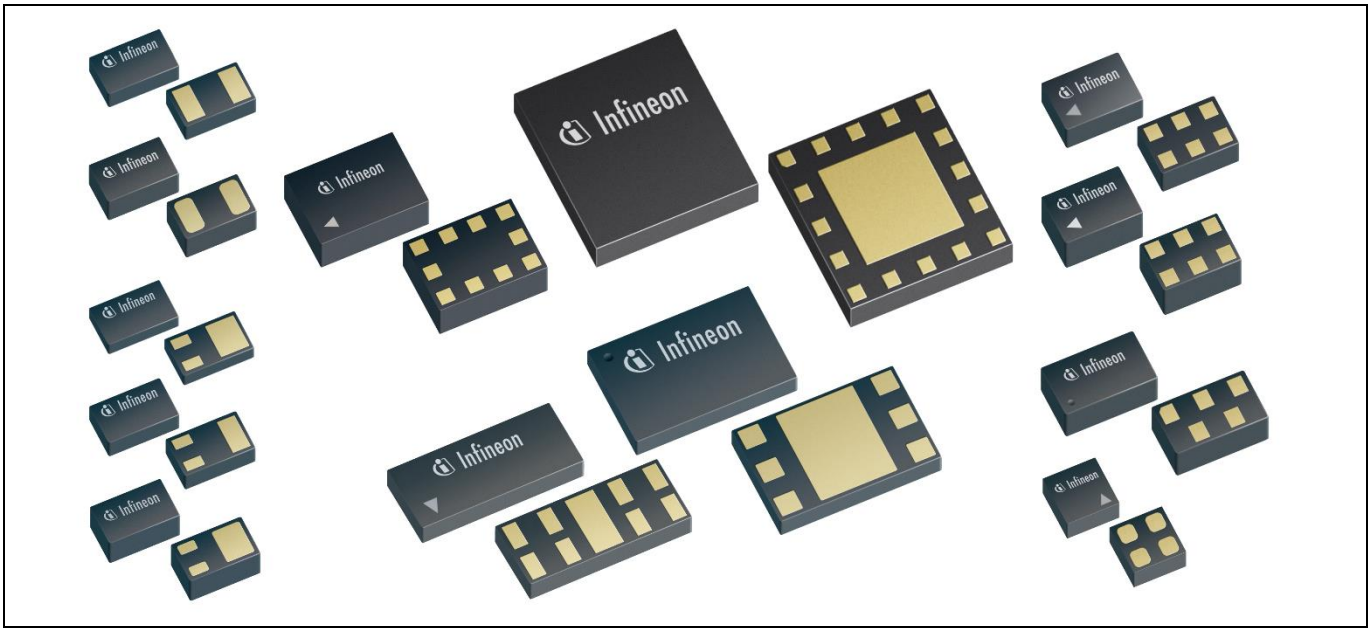

Figure 1 Examples of T(S)SLP packages.

1.2 ATSLP Package Type

Infineon Advanced Thin Small Leadless Packages (ATSLP) have pre-molded compound as a substrate. Internal cuircuits and traces together with via connections are forming a Redistribution Layer (RDL) design. A solder mask layer is defining the Input/Output connections (I/O) and potential exposed pads on the package landing area. **Figure 2** shows examples of the ATSLP.

- PG-ATSLP packages

PG = Plastic Green
A = Advanced
T = Thin
SLP = Small Leadless Package

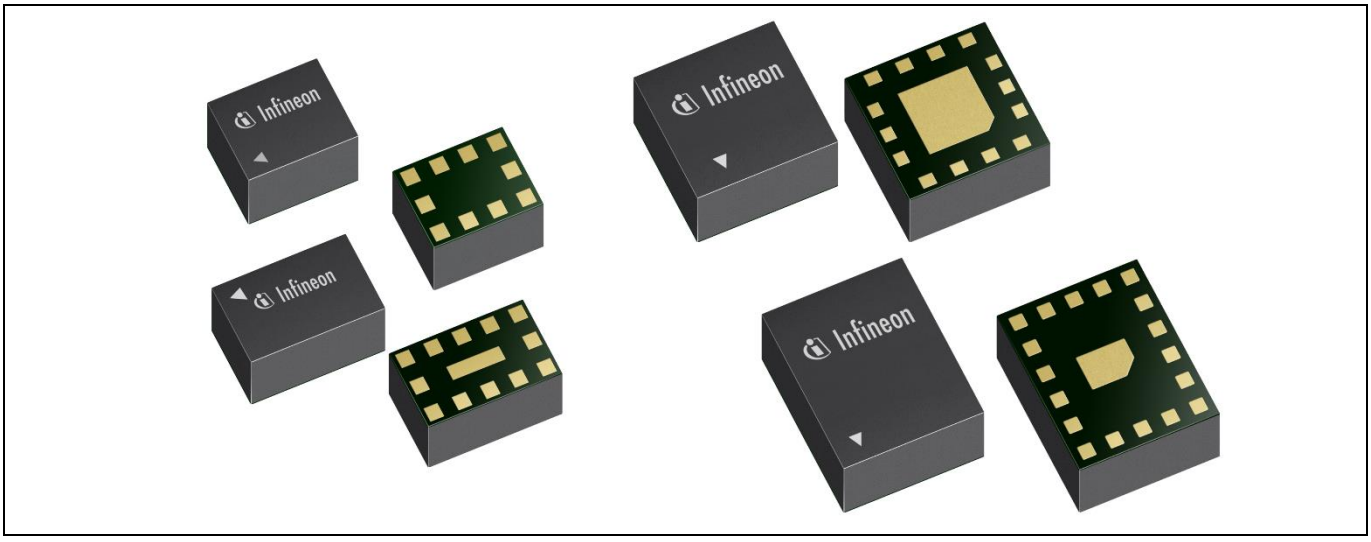

Figure 2 Examples of ATSLP packages.

1.3 LGA Package Type

Land Grid Array packages are built on an advanced laminate substrate with multiple RDL. Thin Fine pitch Land Grid Array packages (TFLGA) feature body thicknesses of down to about 1 mm. Ultra thin profile Land Grid Array packages (ULGA) can reach a thickness below 1 mm. **Figure 3** shows examples of LGA packages.

- PG-TFLGA packages
- PG-ULGA packages

PG = Plastic Green
T = Thin
U = Ultra thin profile
F = Fine pitch
LGA = Land Grid Array

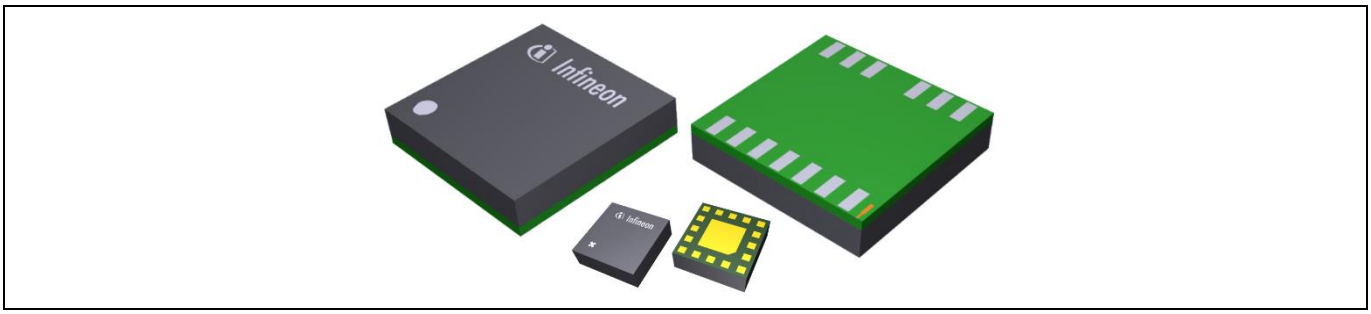

Figure 3 Examples of LGA packages.

1.4 Package Features and General Handling Guidelines

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal Construction

T(S)SLP, ATSLP and LGA offer smallest package dimensions by using an interposer. Multiple die configurations are also possible. All three package types are capable of providing a full array I/O pad configuration at the landing area as well as such having peripheral I/O pads together with thermal or exposed pads. **Figure 4** to **Figure 6** show schematic drawings of the inner setup of the Infineon Thin Small Discrete Packages without Leads.

There is a clear evolution of inner complexity visible. The T(S)SLP package family in **Figure 4** is partially assembled on a copper carrier but features no classical leadframe. The die is either directly connected to the solder pad or by a wire bond. The ATSLP package family in **Figure 5** is using a pre-molded compound as a substrate. That allows to form a RDL. The T(S)SLP as well as the ATSLP family has products with wire bonded dies or flip-chip technology. The LGA package family shown in **Figure 6** allows for high RDL complexity by using a laminate substrate with multiple copper circuitry layers and internal via tracks.

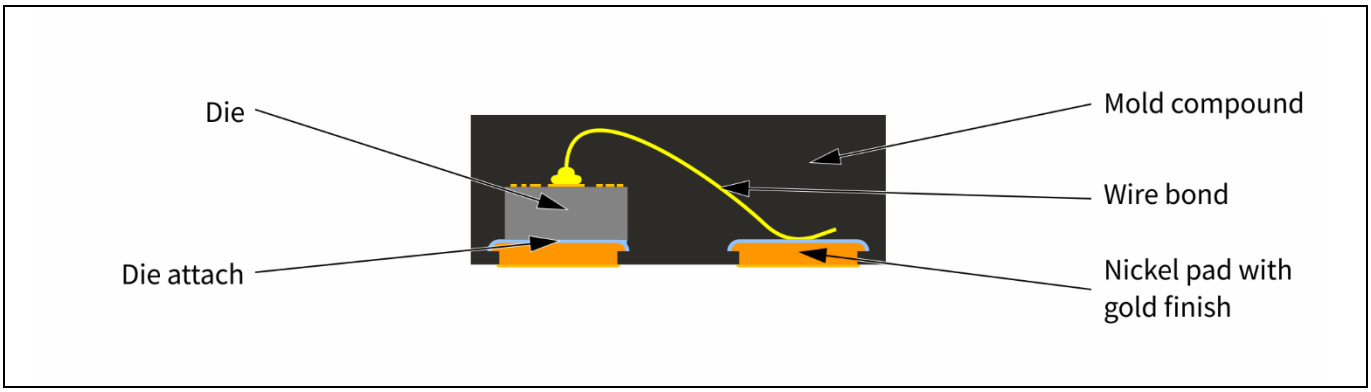

Figure 4 Schematic showing the inner setup of a T(S)SLP with wire bonded die.

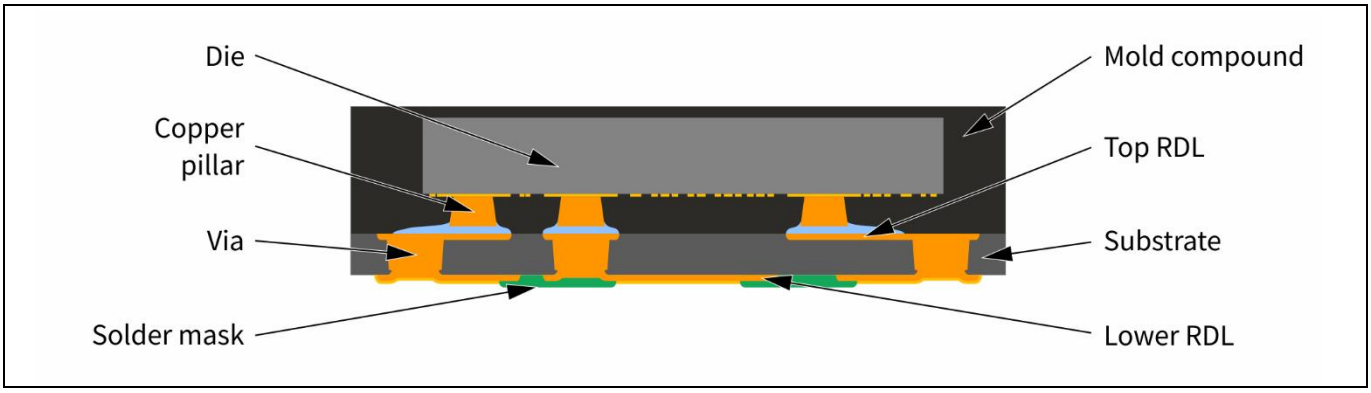

Figure 5 Schematic showing the inner setup of an ATSLP with flip-chip and copper pillars.

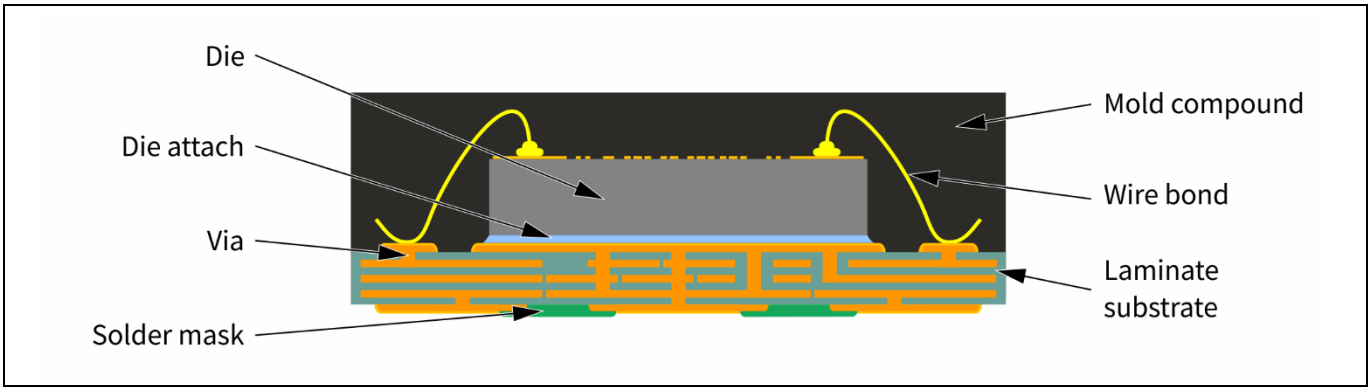

Figure 6 Schematic showing the inner setup of a typical LGA package.

Termination Design

The packages of T(S)SLP, ATSLP and LGA have terminations with a land grid array configuration. The solder joint is consequently formed at the bottom only. **Figure 7** shows a schematic comparison of the different solder joints. The free termination pads of T(S)SLP allow the solder to grip the package pad outline when forming the joint.

The lower RDL of the ATSLP is also forming the landing pattern. The termination pads are registered by solder mask that is left open to the package outline. As a consequence, the pads are partly solder mask defined and partly non-solder mask defined. A typical ATSLP landing area is schown in **Figure 8**. The open solder mask edge allows the solder joint to compensate for volume variations that are naturally caused by the solder paste print tolerances.

When handling ATSLP and LGA special attention should be given to the package to board stand-off. Both of the solder joint partners Printed Circuit Board (PCB) and package can feature a solder mask layer. With sufficient heights, the distance in between the two joining partners can decrease significantly depending on the specific solder paste volume. Solder mask dams in between the PCB landing pads are often stated as being optional.

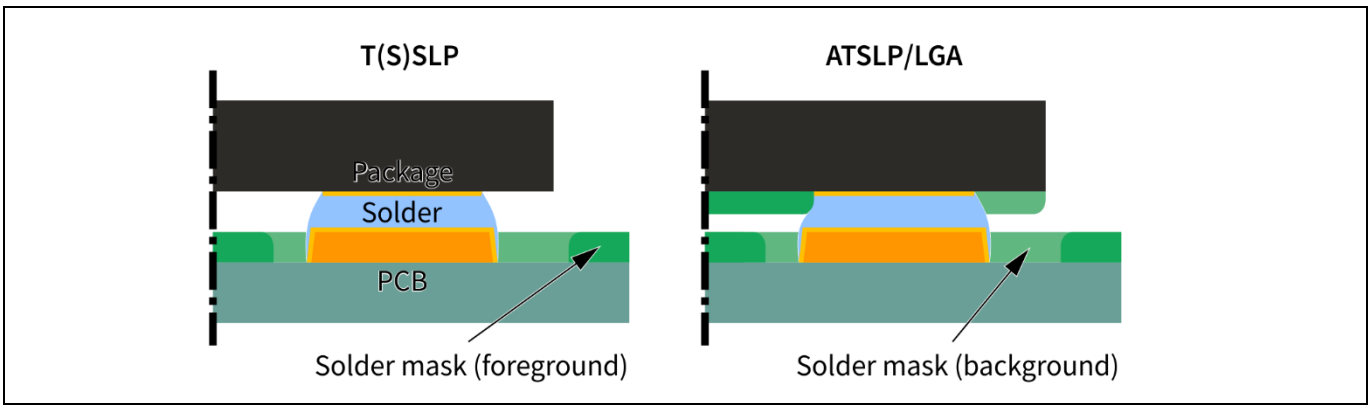

Figure 7 Schematic comparison of T(S)SLP, ATSLP and LGA termination designs. Special attention should be given to the package to board stand-off when having solder mask layers on both joint partners.

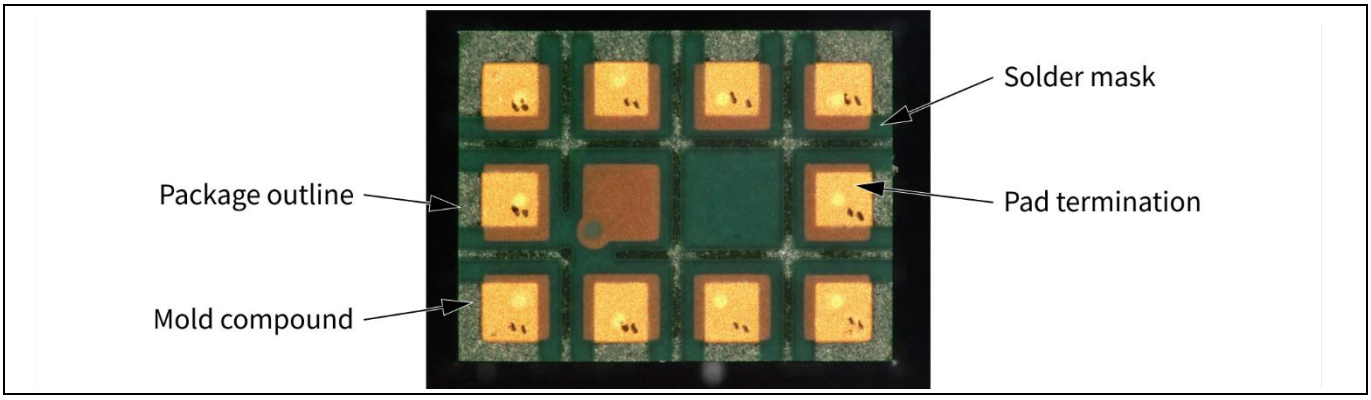

Figure 8 Photograph of an ATSLP landing area. The pad terminations are partly solder mask and non-solder mask defined.

Termination Plating

The final finish of T(S)SLP, ATSLP and LGA terminations consist of nickel/gold (Ni/Au). The sacrificial gold layer dissolves during reflow. The solder connection is then made to the Ni-layer with very stable results in solderability.

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each on top and bottom side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder Mask Defined, SMD or Non-Solder Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

T(S)SLP, ATSLP and LGA have a grid array pad configuration as shown in **Figure 9**. Typicall PCB pads are designed by transferring the package pad outline and circumferentially adding 25 µm. There are application cases where it can be benefical to slightly increase the outwards overhang of the pad outlines. That allows for using stencils with increased thickness and can help to compensate natural stencil printing tolerances. The here discussed PCB pad designs for 2-pin packages must clearly be distinguished from those for passive components (typically resistors or capacitors). Although, they can be classified by their outline dimensions in the same way (e.g. 0201), they feature a different termination geometry type. T(S)SLP, ATSLP and LGA packages feature no wettable sidewalls but are terminated bottom-only. The PCB pad sizes of T(S)SLP, ATSLP, LGA are largely different compared with passive components to provide the optimum solderable area in each case. The recommended PCB pad designs will help to prevent excessive tilting or tombstoning of the here discussed T(S)SLP, ATSLP and LGA packages.

Note: The PCB pad designs for T(S)SLP, ATSLP and LGA packages must not be confused with those for passive components because they do not feature wettable sidewalls but are terminated bottom-only.

The small size of most of the T(S)SLP, ATSLP and LGA packages requires stable geometry tolerances on the PCB. Therefore, the NSMD pad design is recommended. The copper pad tolerances are much lower than those of the solder resist. NSMD pads expose parts of the conductor tracks connecting the pads to the remaining circuitry. The conductor tracks on the PCB should be as narrow as possible (100 µm or less), to minimize the influence by the therefore increased wettable area. Furthermore, only one connection per solder pad with a symmetrical routing, is recommended. Depending on the capabilities of the PCB manufacturer, it might not be possible to separate two NSMD pads by a solder mask dam. The solder mask dams in between the PCB landing pads are therefore often stated as being optional. When having no solder mask dam in between the pads it goes without saying, that the solder paste printing process must be well-controlled.

Centric exposed pads on the landing area of the T(S)SLP, ATSLP and LGA packages are designed to conduct thermal loads into the PCB or to provide a reliable ground connection. Therefore, the exposed pad outline on the PCB should either be congruent with the area on the package or be increased similar to that of the peripheral I/O pads.

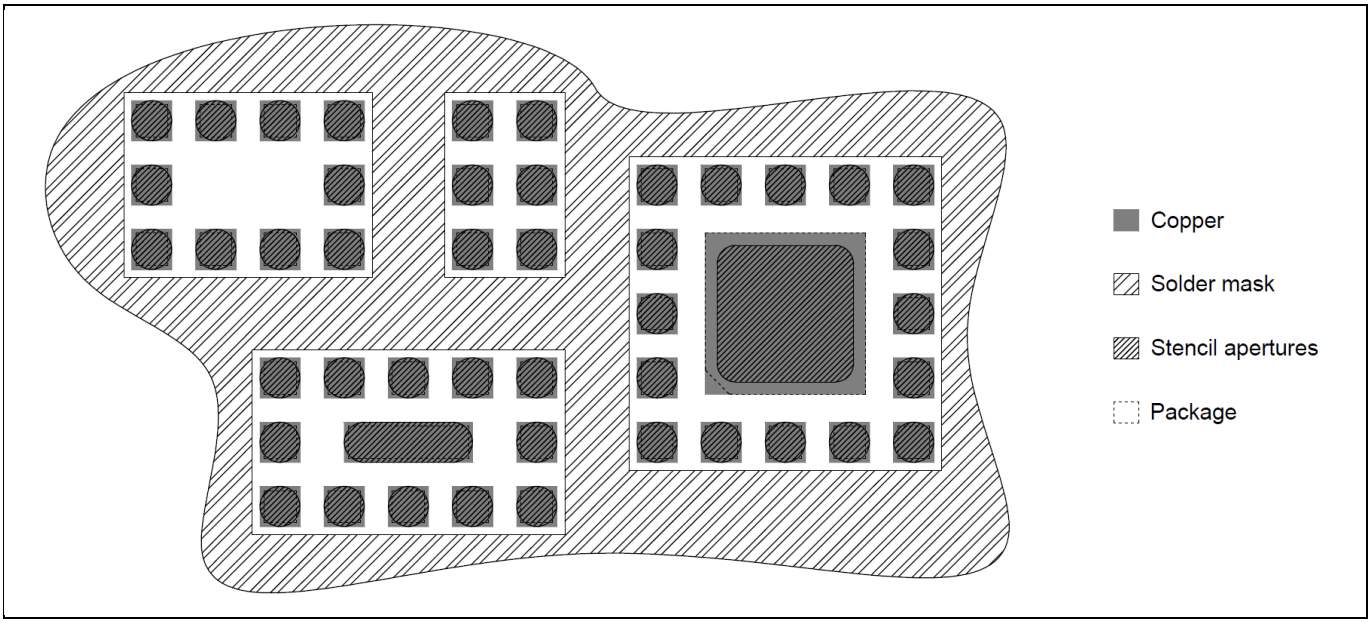

Figure 9 **Example of the land grid array configuration of TSLP, ATSLP and LGA PCB pads. Solder mask dams in between the pads are often stated as being optional. Their use depends on the specific board manufacturing and board assembly processes.**

An optimal PCB design generally depends on the specific application as well as on the specific design guidelines of the chosen board manufacturer.

Further details and specific PCB pad design can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when you are searching the data base. It will then show you an example of the stencil aperture layout for each package. Please also feel free to contact your local sales, application, or quality engineer.

2.3 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat or the electrical signal are then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. The implementation of thermal vias has several impacts on the board assembly processes such as the solder paste print. A constant increase of the number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimum number of vias needed.

Open thermal vias should not be placed under the small T(S)SLP, ATSLP and LGA packages with exposed pad for various reasons. First, the typical hole diameter of open thermal vias is 0.2 - 0.5 mm which is too large to be placed below the small packages in a reasonable array with e.g. 1.0 - 1.2 mm pitch. Second, printed solder can move into the via driven by the wetting forces. Precautionary designs such as placing the via orifice below a stencil beam or covering the orifice with solder mask by “tenting” will most likely not be applicable due to the lack of sufficient space. Consequences of solder penetration can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area, or solder flowing through the via to the opposite side of the PCB.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, open vias can also be placed next to the footprint near the package and be covered with solder mask.

Another alternative is the use of “plugged” microvias. With that method vias 0.2 – 0.1 mm in diameter and smaller are filled with copper, while larger ones are filled with an epoxy. The following overplating step is capable of creating a smooth surface with nearly no discontinuities. They can be placed inside the solder pads and therefore are a preferred solution. It has to be taken care, that also when using plugged vias, the flatness in the pad is crucial to the voiding behavior of the solder joint. Deep dips into the pad have the tendency to trap solder voids.

For further information about vias in pad, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (made of nickel) are preferred. The latter are applied especially when fine-pitch components are assembled.

The stencil apertures for typical T(S)SLP, ATSLP and LGA packages with array configuariton are usually of circular shape having the same extension as the relevant pad on the PCB. Generally rounding the corners of rectangular apertures (radius approx. 50 µm) can support the stencil transfer stability. Stencils with a thickness of typically 80 µm are recommended. TSSLP with package size 0201 stencil thickness ≤ 90 µm should be used based on an area ratio of 0.66. Larger LGA should be assembled using a thickness of up to 130 µm. For

In most cases the thickness of a stencil has to match the needs of all components on the PCB. For the smallest components, however, the solder paste printing process is of specific importance to the quality of the final solder joint. It is therefore recommended to focus specifically on the quality of such prints by facilitating an automated Solder Paste Inspection (SPI). **Figure 10** shows a typical SPI measurement of a solder paste depot for a TSSLP component size 0201.

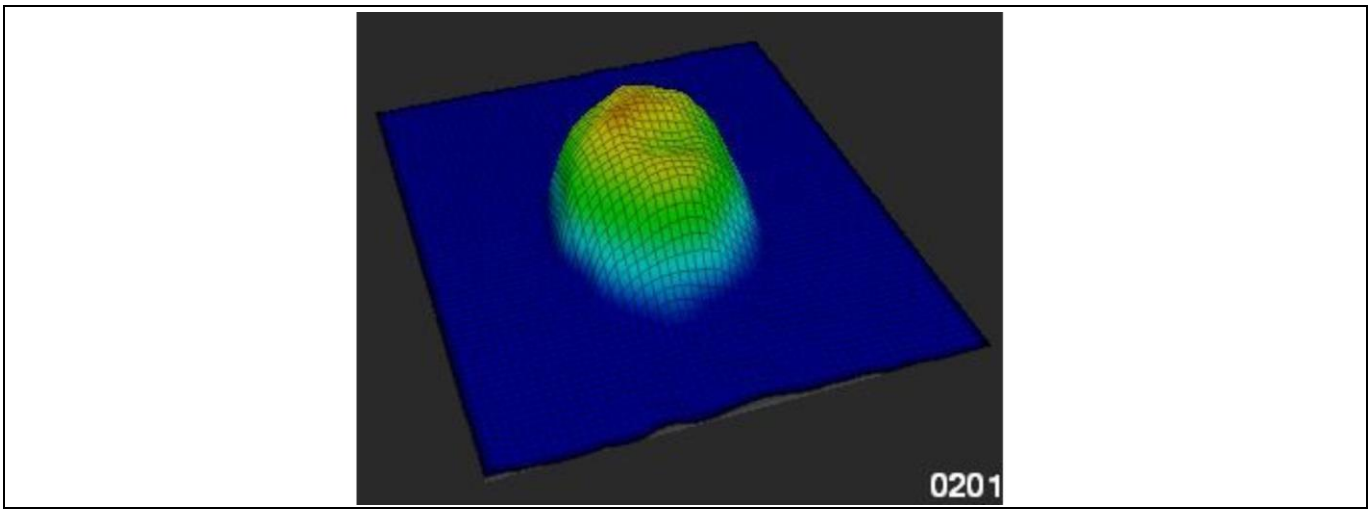

Figure 10 Typical SPI measurement of a solder paste depot for a TSSLP component size 0201.

The reduction of the solder volume that is printed to the pads stabilizes the package during reflow and supports its self-aligning tendency. The print reduction for central exposed pads of TSLP, ATSLP and LGA depends on their difference in size compared with the I/O pads and ranges from 80% to 60% by area.

For individual design adaptations to reach the optimum amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when you are searching the data base. It will then show you an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1% to 4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Using Type 4 paste or higher (with lower grain size of the solder alloy powder) is recommended for the assembly of T(S)SLP, ATSLP and LGA components, depending on the specific stencil aperture size and therefore solder paste transfer efficiency.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For packages where the solder joint is formed mainly on the package bottom side, a “no clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kind of flux residues remain on the board prior to any kind of coating. For power packages, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

The components have to be placed accurately despite the self-alignment effect that is caused by the surface tension of the liquid solder. Positioning the packages manually is not recommended, especially not for packages with small terminations and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the whole PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system prior to the mounting process.

The following recommendations apply especially to the smallest T(S)SLP, ATSLP and LGA packages.

- Especially on large boards, local fiducials close to the device can compensate PCB tolerances.
- The very low tolerances of the T(S)SLP, ATSLP and small LGA package outlines allow the use of outline-referenced alignment as an alternative to the pad-referenced alignment.
- An increased placement force may squeeze the solder paste causing solder joint shorts or beading. Special care must be taken when processing the smallest packages that allow no solder mask dam in between the PCB pads.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

The widely used method of reflow soldering in a forced convection oven is recommended for the PCB assembly of T(S)SLP, ATSLP and LGA components. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the solderability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

T(S)SLP, ATSLP and LGA packages are generally suited for mounting on double-sided PCBs. During the board assembly solder joints of components on the first side will again reflow in the second reflow step. In the reflow zone of the oven (with the solder being in its liquid state), the components are only held in place by wetting forces from the molten solder. Gravity of larger components acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity will force the components closer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, covering a double-sided reflow and one rework cycle. The maximum temperatures must not exceed during application board assembly. Please refer to the product barcode label on the packing material that states the maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

For further information about reflow soldering, please refer to *the General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminations is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

The T(S)SLP, ATSLP and LGA packges with land grid array configuration feature bottom-only terminations. The solder joints are formed underneath the package. A visual inspection of the solder joints with conventional AOI (Automatic Optical Inspection) systems is not possbile. **Figure 11** shows a photograph of typical 2-pin TSSLP solder joints.

Components with 2-pins will show a natural tilt around their long axis. Investigations on the 2nd level reliability have proven that such a tilt does not affect the solder joint lifetime.

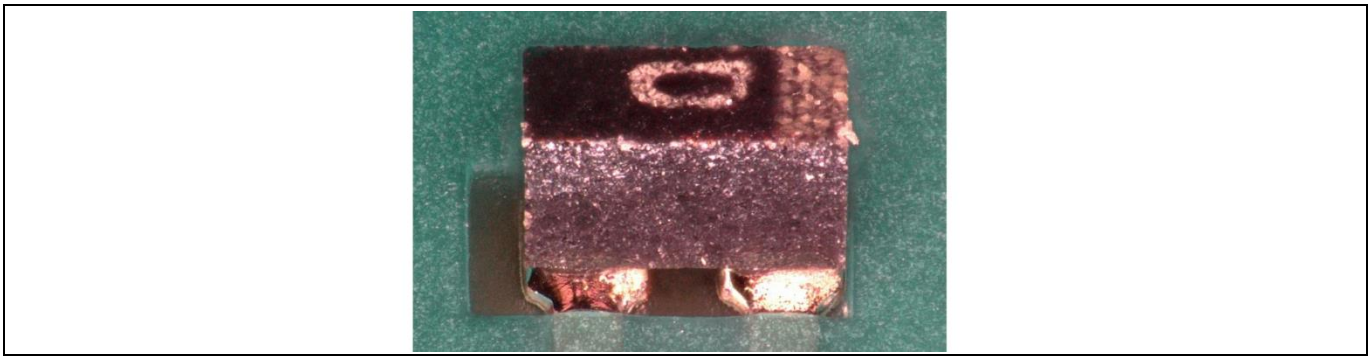

Figure 11 Photograph of typical TSSLP solder joints.

For the acceptability of electronic assemblies, please refer also to the IPC-A-610 standard [6].

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of components that cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspecting, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 12 shows a typical X-ray photograph of a TSLP package. The solder joints, wirebonds, and parts of the package internal setup are visible. Large exposed pads may tend to increase voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the board pad size, the via and stencil layout, the solder paste, and the reflow profile. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

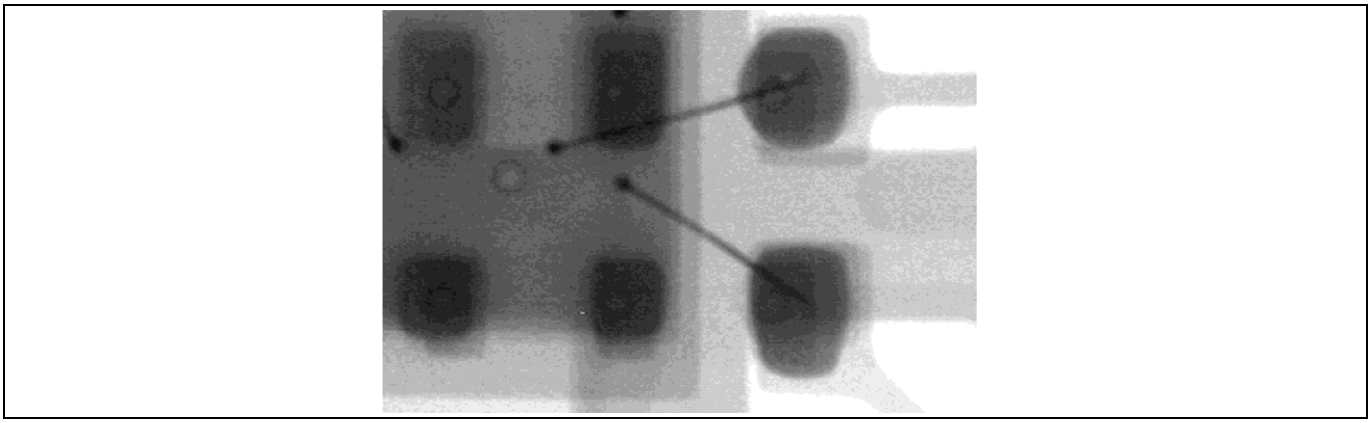

Figure 12 **Typical X-ray image of a soldered TSLP package. The solder joints, bond wires, and parts of the package internal setup are visible.**

6 Rework

Single solder joint repair of packages with land grid array configuration is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to fully automated assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest solution and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (ie onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 6 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

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