Design considerations

Understanding the trade-offs between Si & GaN in high-reliability applications

About this document

Scope and purpose

This document discusses the unique design considerations related to radiation-hardened (rad hard) Si MOSFET and GaN HEMT power devices intended for use in high-reliability space applications. Different aspects of circuit design are discussed that provide rationale to better understand and identify the target applications of Si and GaN.

Intended audience

This document is intended for design engineers and component engineers evaluating power semiconductor design options for high-reliability rad hard applications.

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Table of contents

1 Introduction

The most important aspect of electronics operating in space is reliability. Radiation-hardened (rad hard) devices are different from commercial-off-the-shelf (COTS) parts because they're designed to perform to specification in presence of space radiation. There are numerous variables in which a spacecraft operates and the electrical power system has to deliver consistent and reliable performance. For example, high-energy photons or particles can cause transients, damaging transistors if the voltage across the component exceeds its rating.

From a design perspective, it's crucial to consider the unique considerations and trade-offs between using rad hard Si MOSFET versus GaN HEMT power devices in high-reliability space applications. We'll review different aspects of circuit design to better understand where and when to use Si and GaN.

2 Board layout

Circuit designers spend a great amount of time in optimizing gate-driving circuit and board layout, especially for high-reliability applications. With IR HiRel's rad hard R9 Si MOSFETs, a drop-in replacement can directly show efficiency improvements. For space applications, it is rational to rely on board layouts which are optimized and flight-proven over extended periods, rather than to start a new design.

Inherent to each circuit board and its components, there are associated parasitics: resistance, inductance and capacitance. For example, see Figure 1.

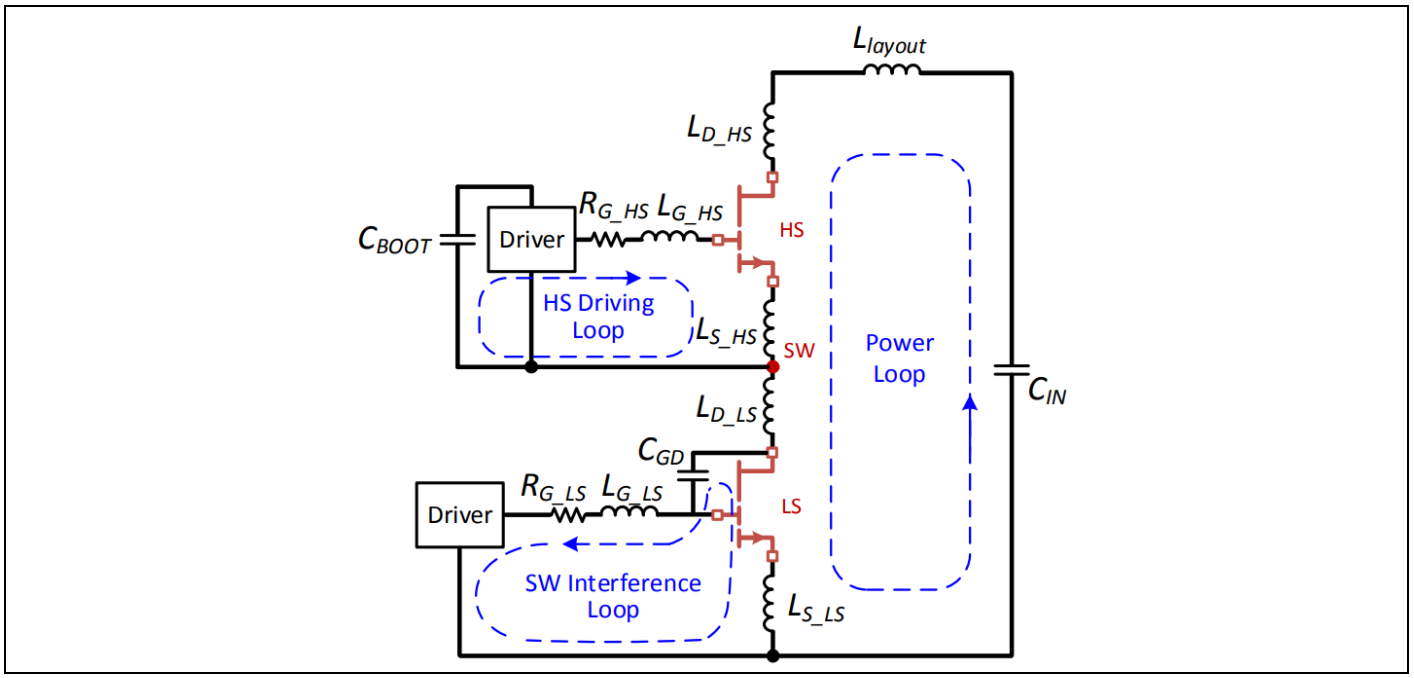

Figure 1 Parasitic elements in buck converter [1]

A 1cm trace on PCB represents parasitic inductance of approximately 10nH. As switching frequency increases, loop inductance becomes a limiting factor in device performance. With decreasing $R_{ds(on)}$, the effect of packaging parasitics also becomes important, as it can affect power converter performance.

During a switching event, there will be a sharp increase or decrease in current which will cause $v = L\frac{di}{dt}$ voltage overshoot across the switch or at the gate of the switch. L can be a parasitic inductance from the power loop or gate driving loop.

For high-switching frequencies, due to the combined effects of high dv/dt and di/dt transitions with low input capacitances and gate thresholds, noise-induced spikes on the gate are observed. Additionally, the Miller effect may result in gate ringing or sustained oscillation. The consequences are false turn-on/off, system malfunction or even device failure. A primary mitigation strategy is to optimize layout such that parasitics are minimal.

Extremely small rise/fall time of switches makes the system more prone to these adverse effects. However, long rise/fall time will result in power losses as energy is dissipated during the switching periods. While switches with extremely small rise/fall time can be used for high switching frequency applications, this comes at a cost of expending more time in test and evaluation of an optimum board layout design.

Table 1 Summary of effects of rise/fall time on circuit

Small rise time (<5ns)	**Larger rise time** (30-200ns)
High-switching frequency operation	Medium-switching frequency operation
Reduces filter size	Relatively larger filter size
Circuit becomes sensitive to parasitics	Circuit is less impacted by parasitics
Costly to optimize board layout	Easy to optimize board layout

Parasitic inductances in the gate driving loop can create a voltage overshoot which may damage the device, especially if the switch is unable to support larger variations in gate-source voltage. The situation is also exacerbated if the switch has extremely small rise time.

For example, GaN devices have rise times of less than 5ns and can only support gate-source voltages from -5V to +6V, making them more susceptible to parasitics. In contrast, IR HiRel's rad hard Si MOSFETs support a strong variation in gate-source voltage (±20V) and have rise times in range of 30-200ns, making them less sensitive to circuit parasitics. By choosing silicon, circuit designers avoid time-consuming design reiterations to minimize gate-source voltage sensitivity to the damaging effects of board parasitics.

IR HiRel's rad hard MOSFETs have sufficiently small rise/fall times and maximum V_{gs} rating of ±20V which provides the designer the benefit of balancing between higher switching frequency, faster time to an optimized board layout design and most importantly – reliability. Through innovative packaging techniques, IR HiRel has built a portfolio of power MOSFETs with different die size having minimum parasitics [2]. With continuous improvement in packaging parasitics, newer generations of Si MOSFETs deliver higher-performance compared to previous ones. For space applications, designers can reuse proven board layout designs and improve performance using newer footprint-compatible Si devices.

3 Safe Operating Area (SOA) – linear mode operation

Si MOSFET are superior, reliable and rugged when operated in linear mode. In linear mode operation, the device functions in the current-saturated region where drain-source current is a function of the gate-source voltage. During switching transitions, switches have to conduct current in presence of drain-source voltage. This is one of the situations where SOA characteristics become important.

SOA plot describes the maximum time a MOSFET can be exposed to a specific voltage and current. There are numerous applications where SOA is extremely important, such as:

- Control circuits including output sequencing, PWM controller and compensation networks
- Pass element for linear regulators
- Protection circuits including input under voltage protection and output over voltage protection, hot-swap/soft-start, short-circuit protection and output turn-off discharge

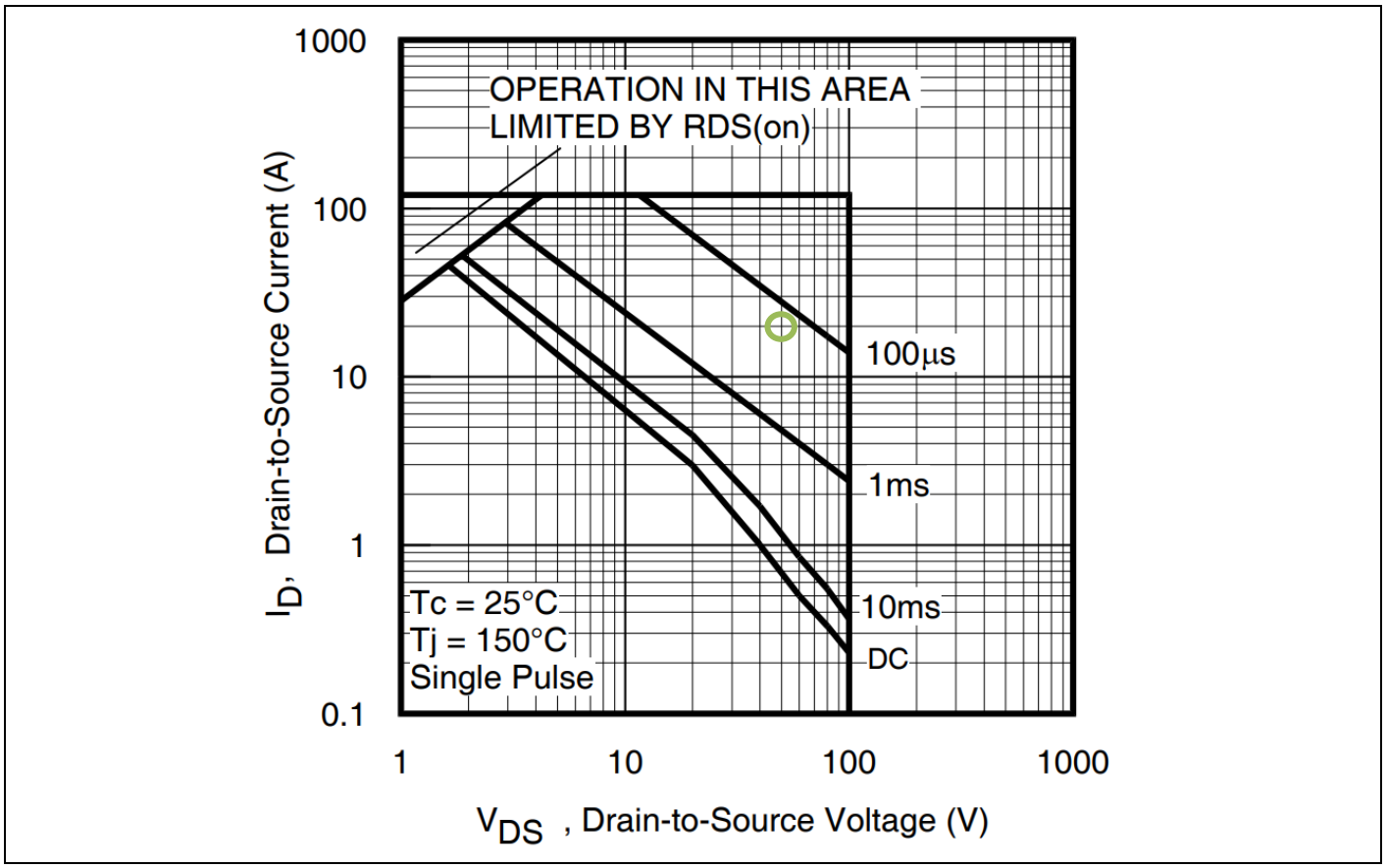

Figure 2 Maximum SOA for 100V, n-channel R9 MOSFET (IRHYS9A7130CM)[3]

In the above SOA plot (Figure 2) of a 100V R9 MOSFET from IR HiRel, if 50V 20A is applied to the MOSFET and the case temperature held at 25°C, then it can operate for at least 100µs without any damage to the device. (For short-duration events, case temperature does not rise significantly). For different applications, the operation limit needs to be defined. When compared with GaN HEMT (Figure 3) for same voltage and current, it can be observed that it can operate without damage for at least 10µs. However, it almost lies at the boundary of SOA for the plot of 10µs

and it cannot support any further increase in current for the same 50V. It can interpreted from this comparison IR HiRel's rad hard Si MOSFET reliability and performance outperforms the GaN device in in linear mode.

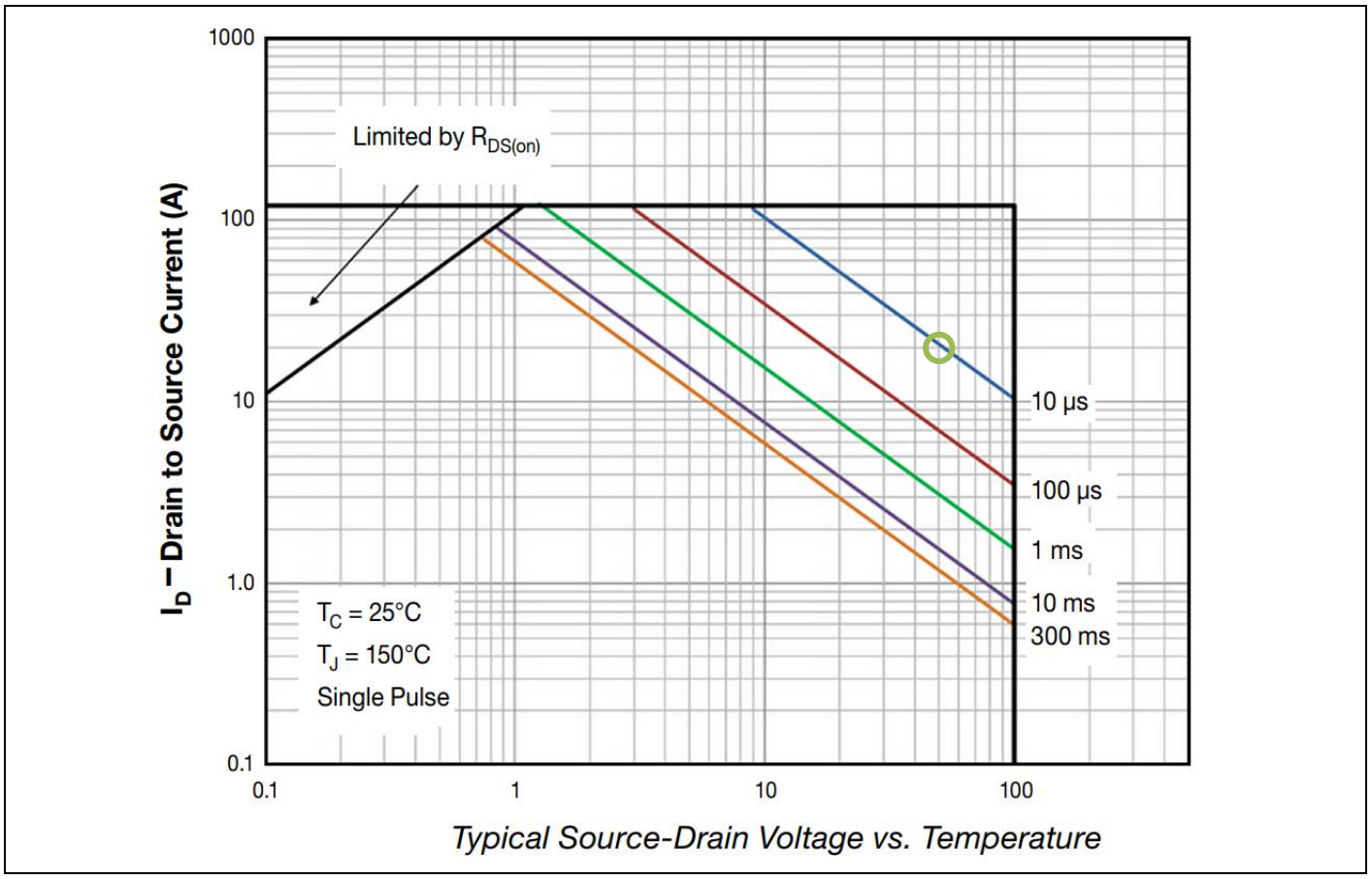

Figure 3 Safe operating area of 100V eGaN HEMT (FBG10N30B [4])

For more information on IR HiRel's rad hard MOSFETs and their operation in linear mode, refer to AN1155[5].

4 P-channel devices

P-channel MOSFETs are often used for load switching. The simplicity of P-channel devices as high-side switches makes them equally attractive for applications such as low-voltage drives and non-isolated point of loads in systems where space is at a premium. The main advantage of a P-channel MOSFET is the simplified gate driving technique in the high side switch position which often reduces the overall cost.

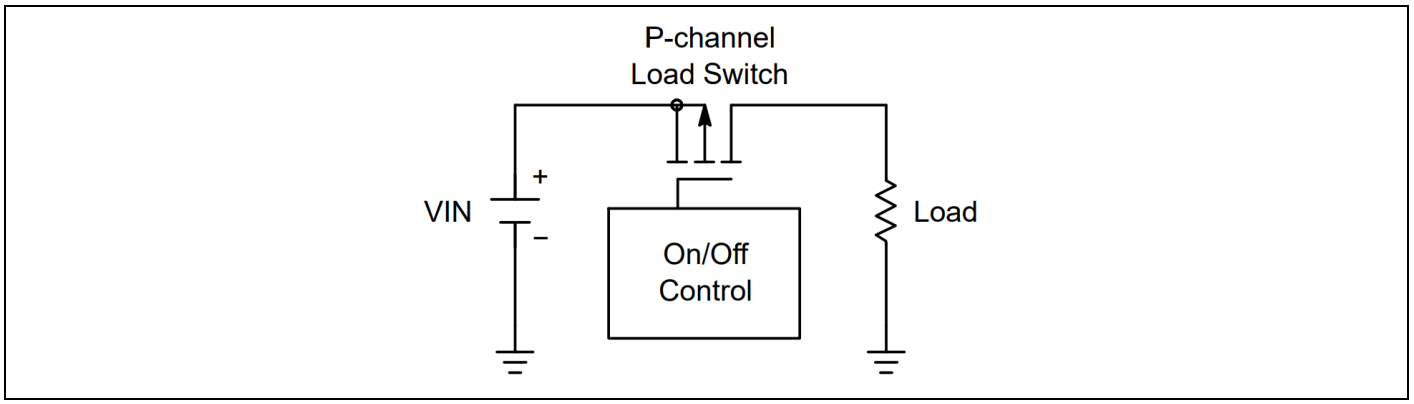

Figure 4 Load switch circuit [6]

In load-switch application,
For N-channel MOSFET,
$V_G \geq V_{OUT} + V_{th}$

For P-channel MOSFET,
$V_{IN} \geq V_G + V_{th}$

where,
V_G = Gate-Voltage
V_{th} = Threshold Voltage
V_{out} = Output Voltage
V_{in} = Input Voltage

To turn on an N-channel device, the gate-voltage must be greater than output voltage. This will require additional biasing supply to raise the gate-voltage higher than output voltage. Compared to this, for a P-channel device, the minimum input voltage must be greater than threshold voltage of the P-channel transistor (which is usually the case). From this, the advantage of P-channel MOSFET over the N-channel MOSFET is apparent. The on/off controller, or gate-driver circuitry, is simpler.

For low-voltage drive applications, a gate driver of an N-channel high side switch requires a bootstrap circuit that creates a gate voltage above the motor voltage rail or an isolated power supply to turn it on. Greater design complexity results in increased design effort and greater space utilization. Similar to load-switch applications, using P-channel MOSFETs can reduce the use of resources here. IR HiRel has the largest portfolio of rad hard P-channel MOSFETs with different packaging options and high-performance in radiation environments.

P-channel devices

Note on depletion mode GaN:
Intrinsically, a GaN device is depletion mode type and normally on. It requires a negative voltage to turn it off. It also needs continuous application of negative supply voltage to keep it off. This might be a problem for certain applications. Commercial devices use N-channel silicon MOSFET in cascode with depletion-mode GaN, to make it "normally-off." The benefit here is that gate drivers available for Si MOSFET can be easily used. However, using the cascode structure introduces the disadvantages of Si MOSFET, including [7]:

- The cascode GaN device will have reverse recovery due to body-diode of Si MOSFET
- Different device structures impact $R_{ds(on)}$
- $R_{ds(on)}$ increases in device with voltage rating < 200V but has very small increase for larger voltage rating (>= 600V)

5 Transient thermal impedance

Transient thermal impedance is important to understand the increase in temperature of the switch when subjected to low frequency, pulsed power. Thermal resistance from junction-to-case (θ_{jc}) determines the temperature increase of the transistor.

$T_{junction} = T_{case} + \theta_{jc} * P_{dissipated}$

In the following, R9 MOSFET and eGaN HEMT with similar voltage and maximum power dissipation are compared. θ_{jc} for Si MOSFET is 21% smaller than eGaN HEMT. This means Si MOSFET can dissipate 1.25x power than its GaN counterpart. For 1ms, 50% duty pulse, following calculations are done:

From the plot below (Figure 5) of 100V, N-Channel, R9 MOSFET:

$\theta_{jc} \approx 1.2\ ^{\circ}C/W$

$T_{junction(max)} = 150\ ^{\circ}C$

$T_{case} = 25\ ^{\circ}C$ (assuming)*

Maximum power that the device can dissipate = $\frac{T_{junction(\max)} - T_{case}}{\theta_{jc}}$ = 104.17 W

*For power pulse of duration longer than 10ms, case temperature needs to be appropriately derated/increased in order to obtain actual power.

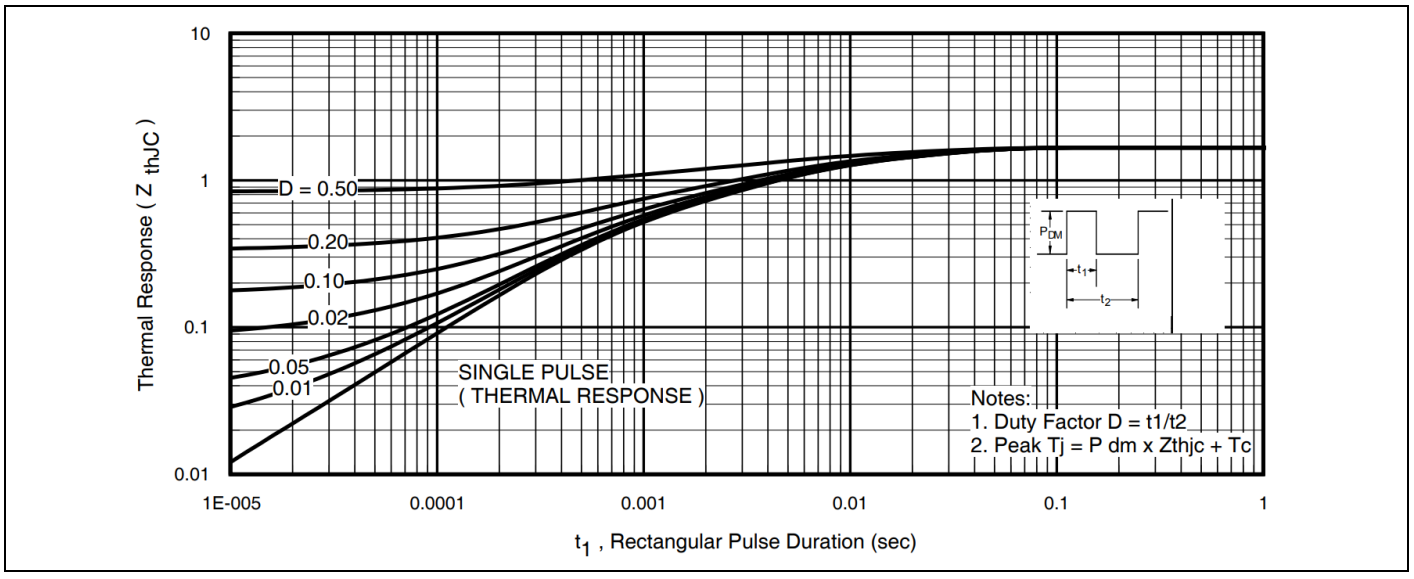

Figure 5 Maximum transient thermal impedance of a 100V, n-channel R9 MOSFET (IRHYS9A7130CM)

From the plot below (Figure 6) of 100V, eGaN HEMT

Transient thermal impedance

$\theta_{jc} \approx 1.5\ ^{\circ}C/W$

$T_{junction(max)} = 150\ ^{\circ}C$

$T_{case} = 25\ ^{\circ}C$ (assuming)

Maximum power that the device can dissipate = $\frac{T_{junction(\max)} - T_{case}}{\theta_{jc}} = 83.33\ W$

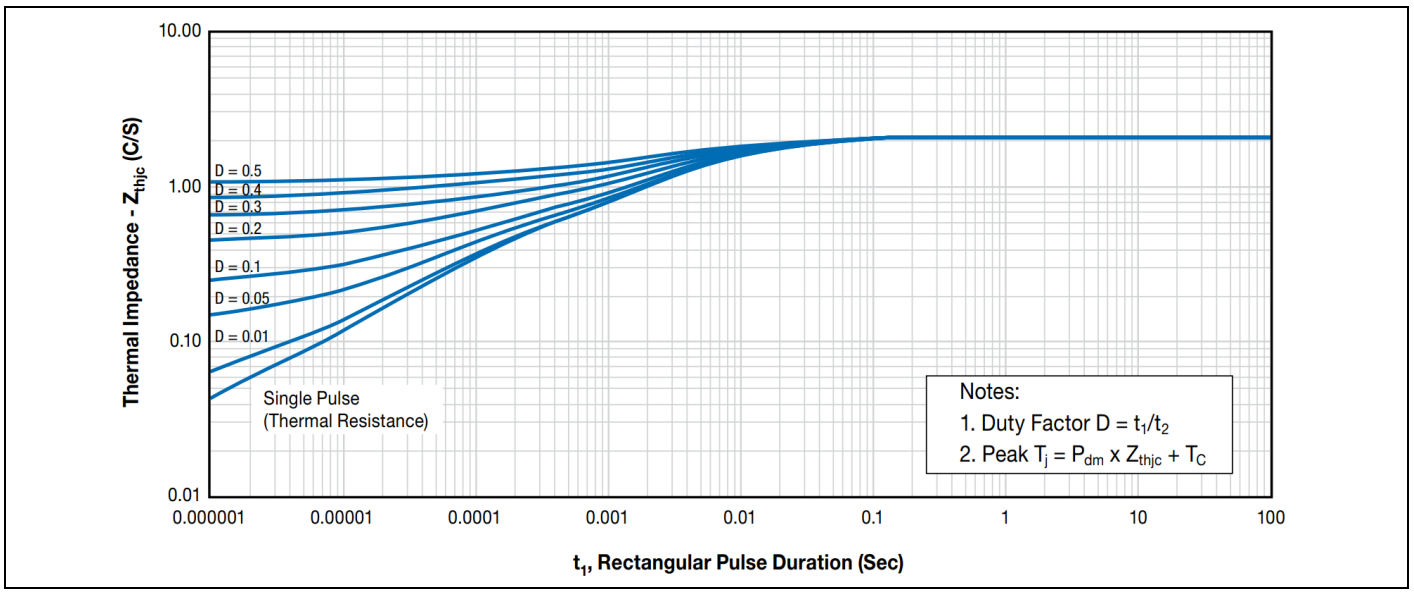

Figure 6 Maximum Transient Thermal Impedance of a 100V, eGaN HEMT (FBG10N30B)**

From this comparison, it can be concluded that the Si MOSFET can dissipate 25% more power than the GaN counterpart without exceeding its rating.

6 Avalanche effect

A power MOSFET can experience voltage overshoot due to turn-off of inductive load or stray inductance present in the circuit. If this voltage exceeds the specified breakdown voltage rating BV_{DSS}, an avalanche current will flow through the device. The switch will be able to operate above its breakdown voltage and can return to normal operation, if the junction temperature of the switch is not exceeded during this event. If a Single Event Transient (SET) due to radiation or due to battery/load issue occurs, then the controller will try to turn-on/turn-off switches instantly. If there is an inductor or parasitic inductance that is in series with the switch then this event will cause a $v = L\frac{di}{dt}$ voltage spike across the switch (See Figure 7). This is considered in worst-case scenarios while designing however the voltage rating can be exceeded. IR HiRel's rad hard MOSFETs are designed to absorb more amount of avalanche energy such that the device is able to withstand short pulses of overshoot in drain-source voltage.

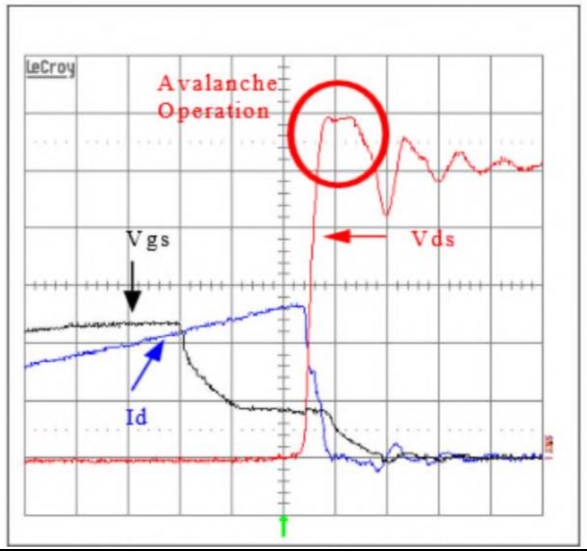

Figure 7 Si MOSFET in a flyback converter under avalanche waveform [8]

Performing under a sensitive environment is critical where it is not possible to replace parts if they get damaged. Redundancy is commonly used in space applications and it comes with a heavy cost. Losing one power supply immediately deteriorates the lifetime of the spacecraft. It is never an intent to stress the device to their extremes and for longer duration. It is important to make sure device operates below its maximum rating under all operating conditions including worst-case scenarios. Absorbing higher amount of avalanche energy makes Si MOSFETs rugged. It is more practical to prefer a device that withstands voltage overshoot than a device which does not* have the capability to operate above its maximum rating.

* GaN has higher dielectric breakdown voltage beyond its absolute maximum rating. However for lower voltage GaN devices, the margin is very small.

E.g. In datasheet of EPC2045,

Drain-to-Source Voltage (Continuous): 100V

Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C): 120V

600V GaN (IGO60R070D1) has 800V dielectric breakdown voltage. But these are not available yet as rad hard. So GaN is more rugged at higher voltage, but the margin is limited for lower voltage devices, making Si MOSFET a better choice for low voltages, especially for rad hard applications.

7 Conclusion

Silicon devices have flight-proven heritage in space, known industry standards for qualification and screening, and are well-understood for use in high-reliability applications. New silicon MOSFET platforms, such as R9, and packaging innovations like SupIR-SMD [9], enable higher degrees of efficiency, reliability and design reuse of proven circuit blocks.

GaN devices have different device structures and less understood failure mechanisms. As such, there are currently no industry standards to screen and qualify GaN for use in rad hard applications. Although they can potentially surpass Si MOSFET performance in terms of power density and TID rating, power systems designers need to balance the trade-offs. Wide adoption of GaN in space applications will require extensive design and test efforts for gate-driver design, reduction of circuit parasitics, radiation-induced failure testing and other design modifications. Optimization of overall electrical system design will require use of both Si and GaN devices having distinct advantages in terms of reliability and performance.

8 References

[1] X. e. a. You, "A Gallium-Nitride Point-of-load DC-DC Converter for Space Applications," in *European Space Power Conference (ESPC), IEEE*, 2019.

[2] D. O. R. F. C. A. M. E. a. P. M. T. Meade, "Parasitic inductance effect on switching losses for a high frequency Dc-Dc converter," in *Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Austin, TX, 2008.

[3] "Datasheet IRHYS9A7130CM," [Online]. Available: http://www.irf.com/product-info/datasheets/data/irhys9a7130cm.pdf.

[4] "Datasheet FBG10N30B," [Online]. Available: https://epc.space/documents/datasheets/FBG10N30B-datasheet.pdf.

[5] M. F. Thompson, "AN-1155 Linear Mode Operation of Radiation Hardened MOSFETS," [Online]. Available: http://www.irf.com/technical-info/appnotes/an-1155.pdf.

[6] "AND9093/D Using MOSFETs in Load Switch Applications," [Online]. Available: https://www.onsemi.cn/PowerSolutions/document/AND9093-D.PDF.

[7] S. Chellappan, "Design considerations of GaN devices for improving powerconverter efficiency and density," November 2017. [Online]. Available: https://www.ti.com/lit/wp/slyy124/slyy124.pdf.

[8] "Application Note AN-1005," [Online]. Available: https://www.infineon.com/dgdl/an-1005.pdf?fileId=5546d462533600a401535590ab660f3a.

[9] J. D. M. F. T. Shunhe Xiong, "AN-1222 The SupIR-SMD, A New IR HiRel Surface Mount Device Package," [Online]. Available: http://www.irf.com/technical-info/appnotes/an-1222.pdf.

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