Customer Training Workshop

Traveo™ II Sound Generator

Q4 2020

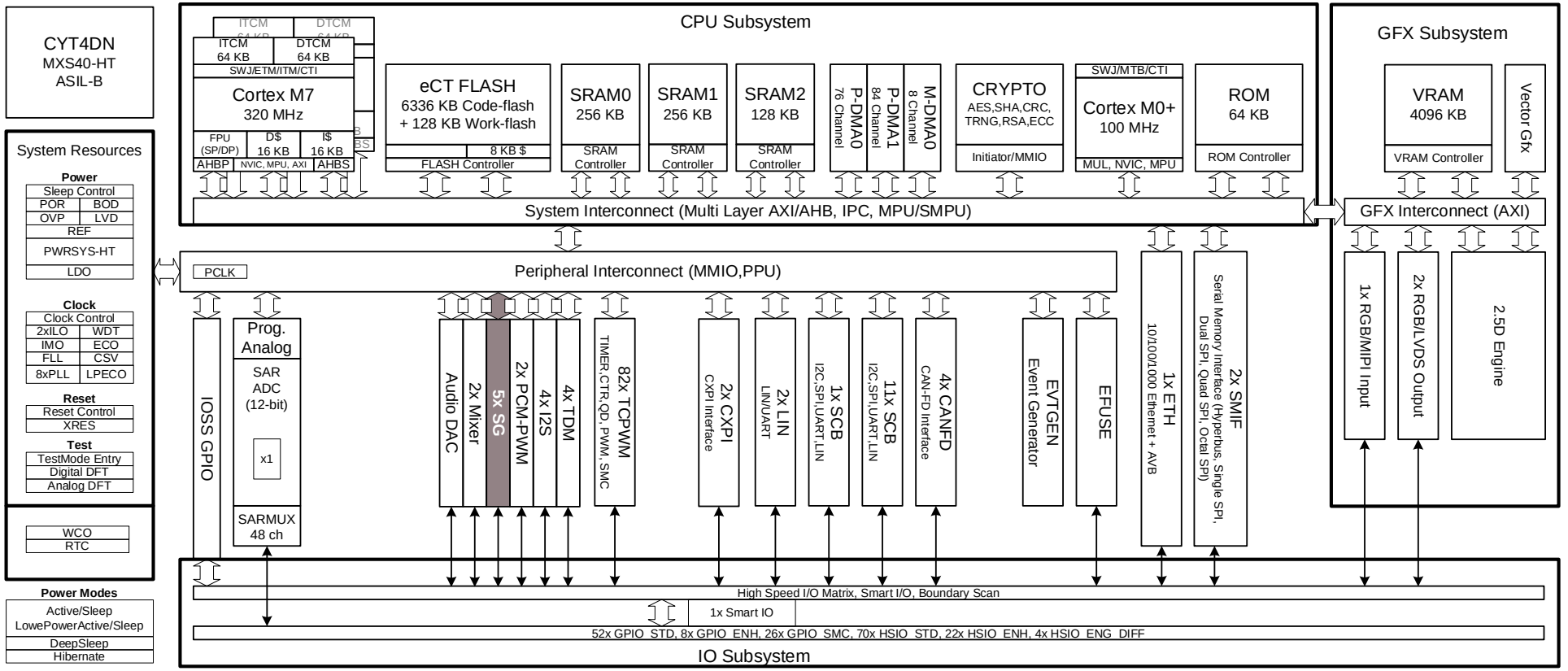
Target Products

› Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo™ II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Cluster

› The Sound Generator (SG) is part of Peripheral Blocks



Hint Bar

Review TRM chapter 33 for additional details

Sound Generator (SG) Overview

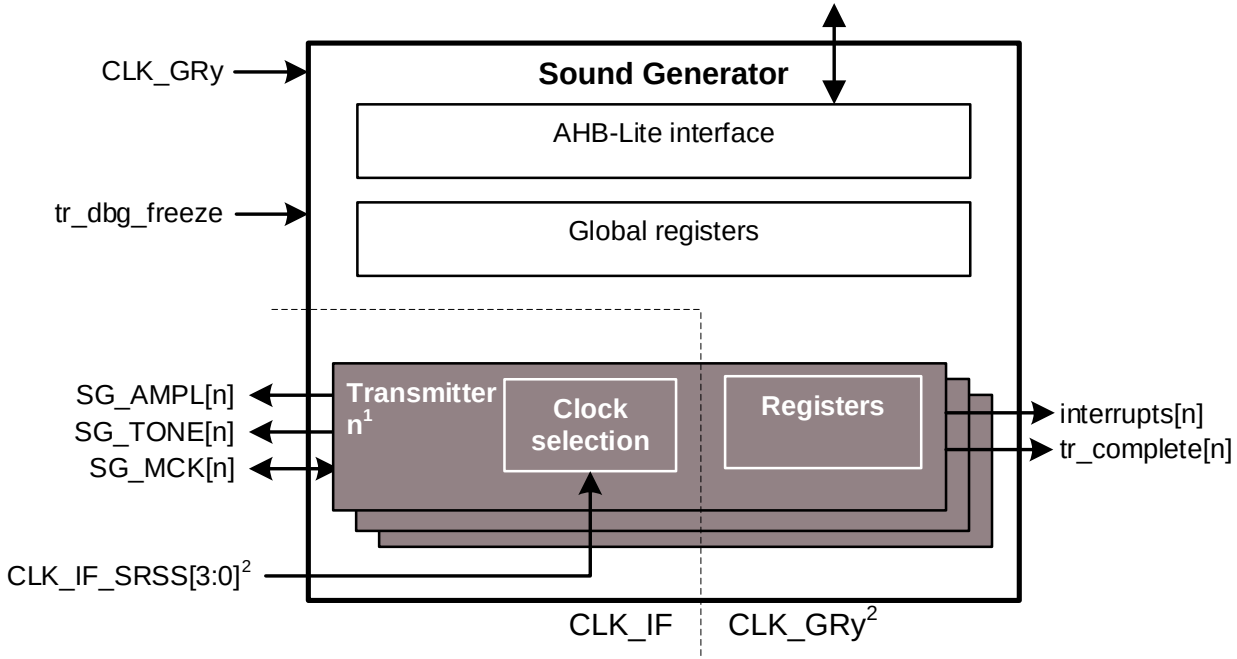
- SG produces PWM tone and amplitude signals
  - Tone signal is used to generate sound frequencies
  - Amplitude signal is used for volume control
- Features
  - PWM-modulated (amplitude, tone) sound generation
  - Double-buffered segment structure control
  - Two operating modes
    - Separate volume and frequency control (two signals) format
    - Combined volume-frequency control (one signal) format
  - Programmable interface clock

Hint Bar

Review TRM section 33.5 for additional details

SG Block Diagram

- SG components
  - Transmitter block
  - Clock
  - Output signals and segment structure
  - Double buffering
  - Audio waveform composition
  - Interrupt



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Review TRM section 33.5.2 for additional details

CLK_GR: Clock input to peripheral functions, which is grouped by the clock gater

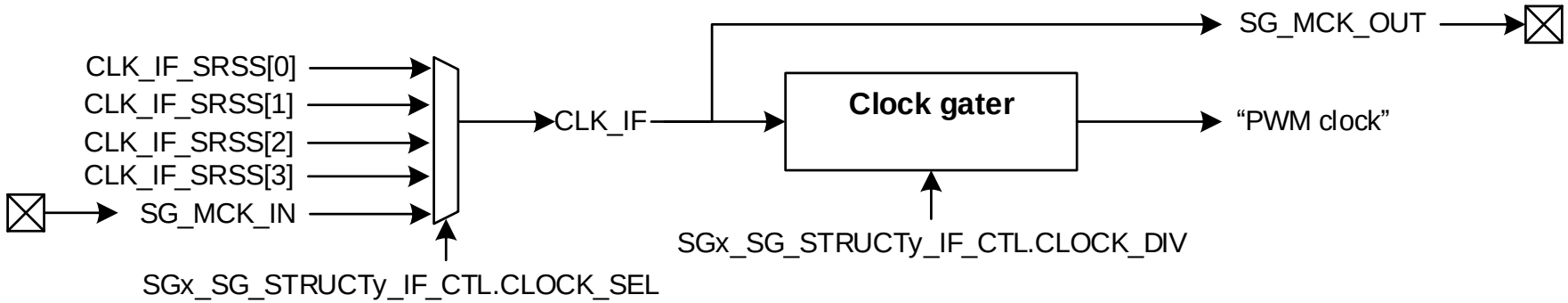
[1] Number of transmitters (n) varies by device
[2] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy

PWM Interface Clock

- PWM interface clock can be derived from either of these clock signals

Signal	Description
CLK_IF_SRSS[3:0][1]	SRSS clock
SG_MCK_IN	Master interface clock

- An interface clock (CLK_IF) is derived and then gated to derive the PWM clock



- PWM clock drives the SG_AMPL_OUT and SG_TONE_OUT lines and its resolution determines the amplitude PWM period frequency

[1] See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0]

Hint Bar

Review TRM section 33.5.3 for additional details

SG_AMPL_OUT: Amplitude output

SG_TONE_OUT: Tone output

Review the Clock System Training section for additional details about high-frequency clocks

Output Signals and Segment Structure (1/2)

- SG creates amplitude signals (SG_AMPL) and PWM tone signals (SG_TONE)
  - Amplitude determines how loud the sound will be
  - Tone determines the pitch of the sound
- To control the output of SG_AMPL and SG_TONE, SG uses four 32-bit segment structure registers

Segment Structure	Description	Register
Amplitude	Specifies the volume of the sound	AMPL_CTL
Tone	Specifies the frequency of the sound	TONE_CTL
Time	Specifies how long a certain tone is played	TIME_CTL
Step	Specifies whether the volume is constant, decreasing, or increasing	STEP_CTL

Hint Bar

Review TRM section 33.5.4 for additional details

Review Registers TRM for additional details

Output Signals and Segment Structure (2/2)

- Segment structure

① A single amplitude period is (AMPL_CTL.PERIOD + 1) PWM clock cycles

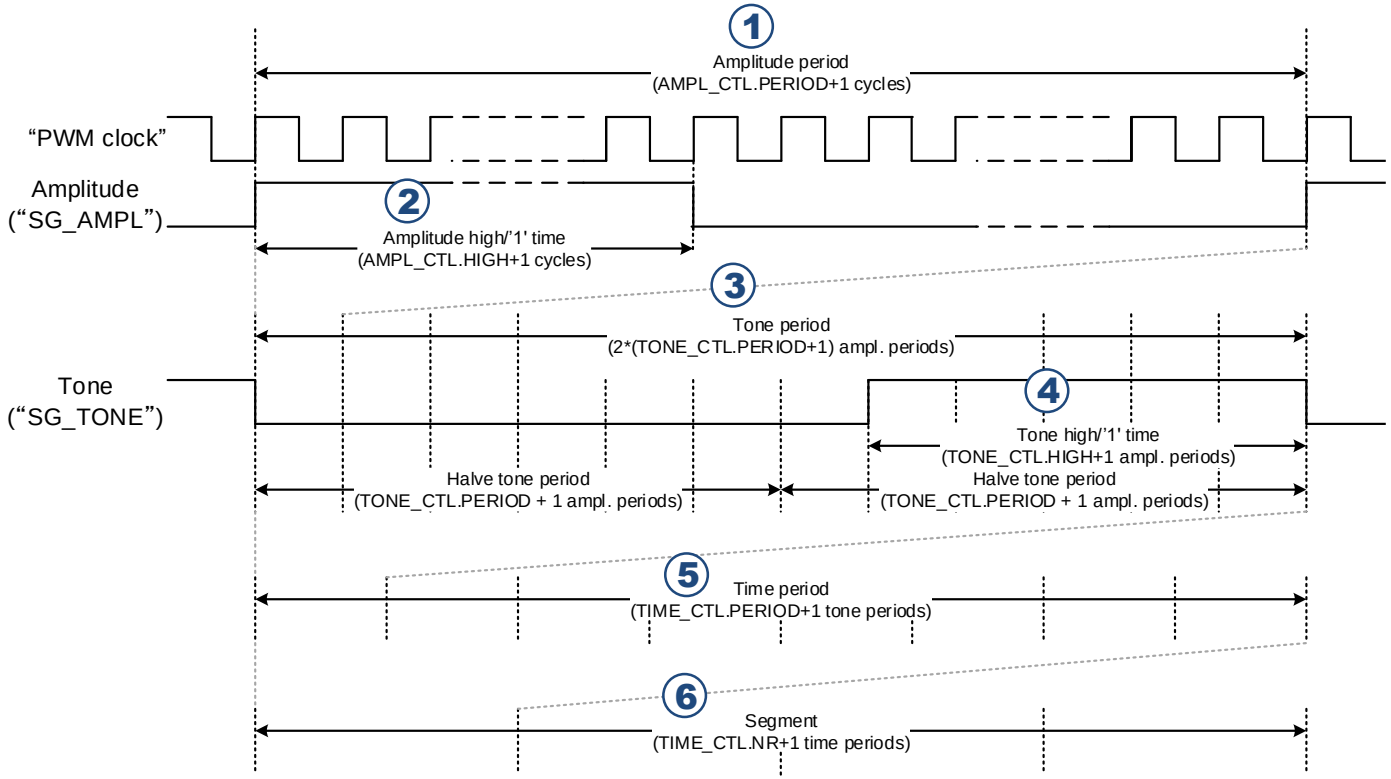
② The high time of an amplitude period is specified by (AMPL_CTL.HIGH + 1) PWM clock cycles

③ A single tone period is two times the (TONE_CTL.PERIOD + 1) amplitude periods

④ The high time of a tone period is defined by (TONE_CTL.HIGH + 1) amplitude periods

⑤ A single time period is (TIME_CTL.PERIOD + 1) tone periods

⑥ A single segment is (TIME_CTL.NR + 1) time periods



Double Buffering

- To generate sound continuously, double-buffered structures are used
- Current structure can control the sound generation process
- Buffered structure can be updated by a CPU or P-DMA
- When the current structure is complete, a completion event is activated, and the buffered structure is copied to the current structure

Hint Bar

Review TRM section 33.5.5 for additional details

[1] Excluding Start bit or Stop bit

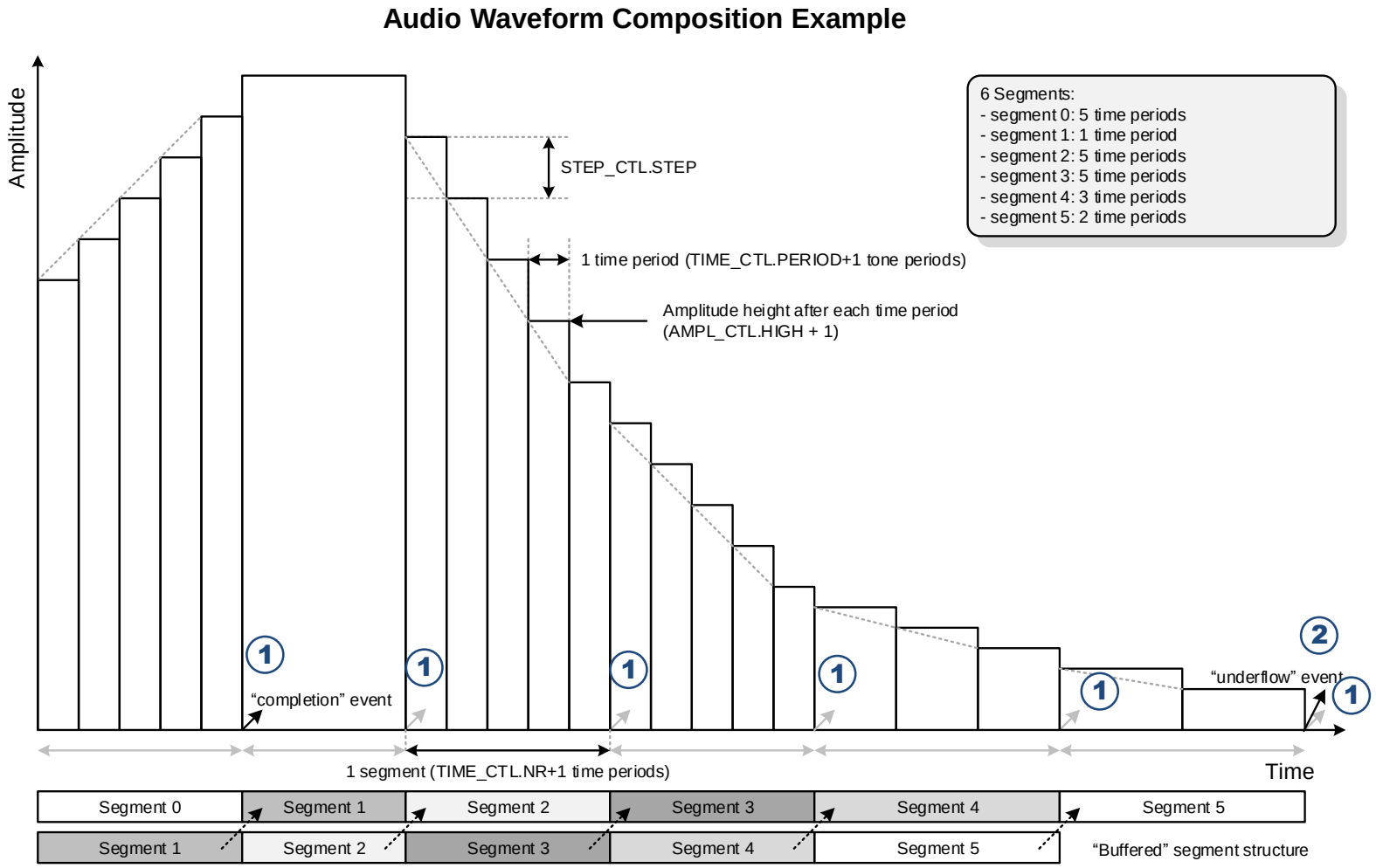
Audio Waveform Composition

- In the diagram, multiple segments are used to describe a sound signal
- After each segment, hardware

① Activates a completion event that
  - Updates the current segment's structure with information of the buffered segment structure
  - Activates tr_complete trigger
  - Activates INTR_TX.COMPLETE interrupt cause

② If the completion event is not followed by a buffered segment structure, it activates an underflow event and the sound generation ends

Audio Waveform Composition



Interrupt

› A sound generator interrupt can be triggered by any of the following events

Interrupt	Set Condition
INTR_TX.COMPLETE	A segment descriptor is complete
INTR_TX.UNDERFLOW	A new segment structure is not available
INTR_TX.IF_UNDERFLOW[1]	Sample pairs (amplitude, tone) are not generated in time for the interface logic. It may indicate that the SG block system frequency is too low with respect to the interface frequency (a SW configuration error)

Hint Bar

Review TRM section 33.5.4 for additional details

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002-27875 *B, 2020-12-24

Revision History

Revision	ECN	Submission Date	Description of Change
**	6638977	07/29/2019	Initial release
*A	6805395	02/12/2020	Added note descriptions in each slide
*B	7053619	12/24/2020	Updated page 2, 5, 6