QSPI
Queued Synchronous Peripheral Interface

AURIX™ TC3xx Microcontroller Training
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Infineon

QSPI
Queued Synchronous Peripheral Interface
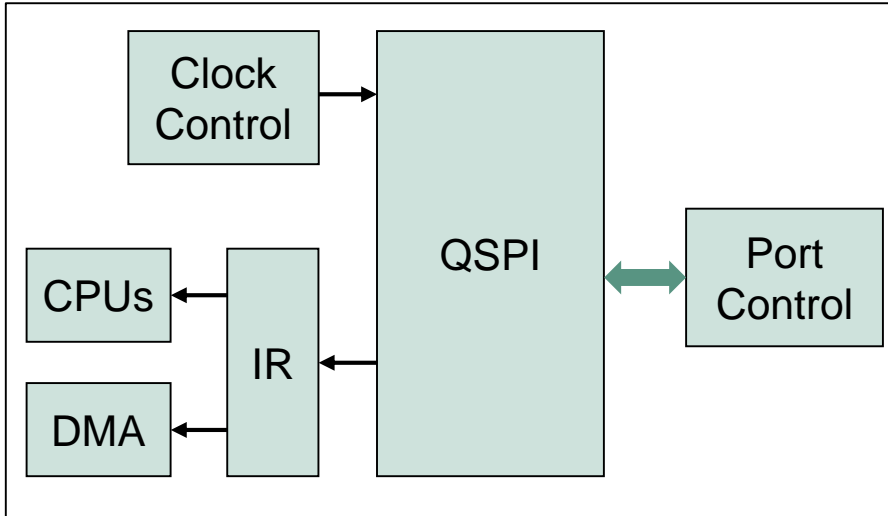
Highlights

QSPI module provides synchronous serial communication with external devices using clock, data-in, data-out and slave select signals.

› Master and Slave full duplex operation

› Up to 50 Mbit/s

Key Features

Queue support

Flexible frame format

Customer Benefits

› Configuration and data via the same Queue (Tx or Rx FIFO)

› Configurable shift direction, clock polarity and phase

QSPI
Queue support

› The Tx-FIFO could keep the data to be sent and additionally the configuration data for the SPI module

› This enables dynamic and comfortable switching of SPI frame timings and data configuration independent for each channel:

- Data length

- LSB/MSB shift first

- Clock polarity and clock phase

- Flexible baud rates and delays

- Parity Type

- Flexible frame length

QSPI
Flexible frame format
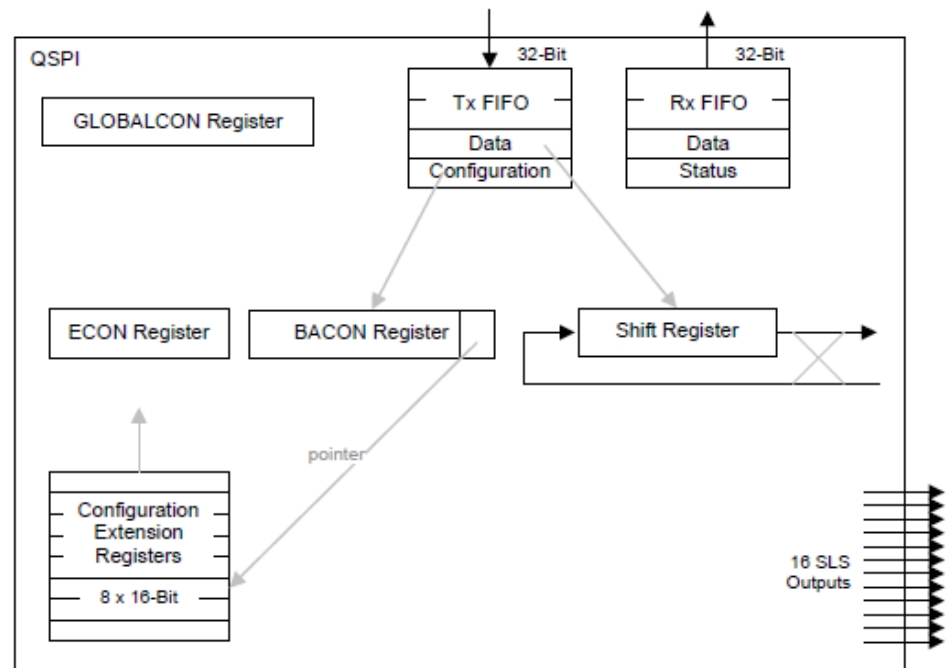
› Programmable number of data bits: 2 to 32 data bits (plus parity: 3 to 33 bits)

› 4 to 32 data bits possible for 50 Mbit/s

› Programmable shift direction: LSB or MSB shift first

› Programmable clock polarity: Idle low or idle high state for the shift clock

› Programmable clock phase: data shift with leading or trailing edge of the shift clock

› Flexible baud rate and delays (leading, trailing, idle) generation
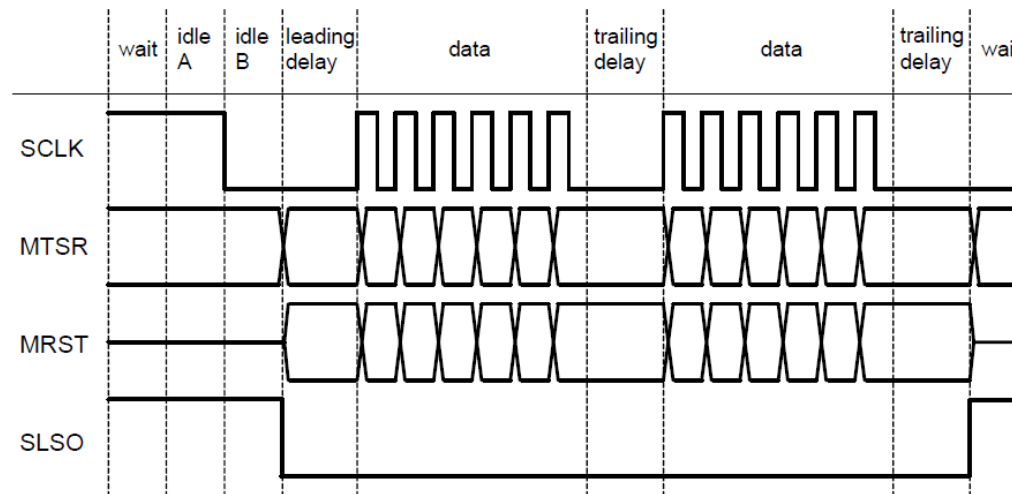
QSPI
System integration

› FIFOs can be handled by DMA controller

› Interrupt generation on

  – transmitter FIFO event

  – receiver FIFO event

  – error condition

  – phase transition

› Seven slave select inputs SLSI in Slave Mode

› Sixteen programmable slave select outputs SLSO in Master Mode
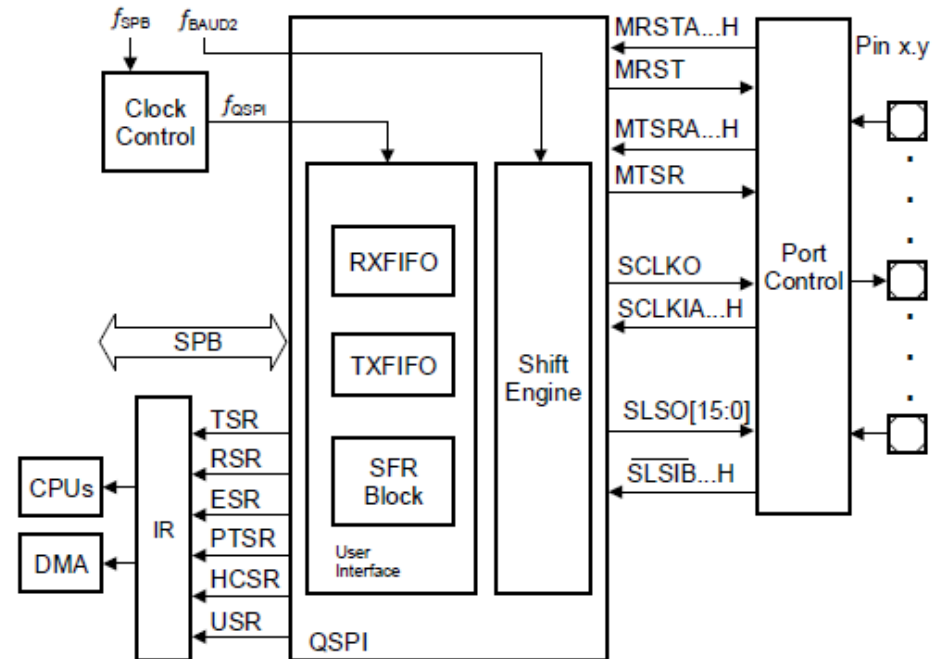
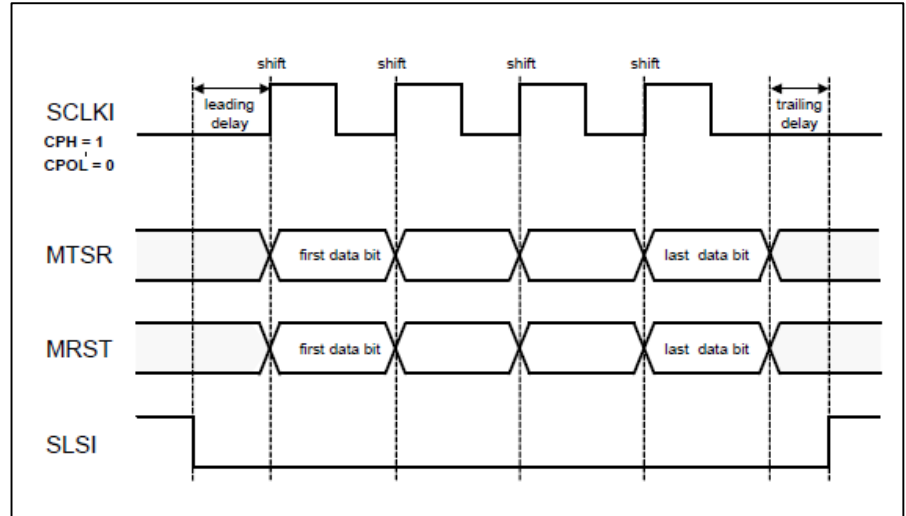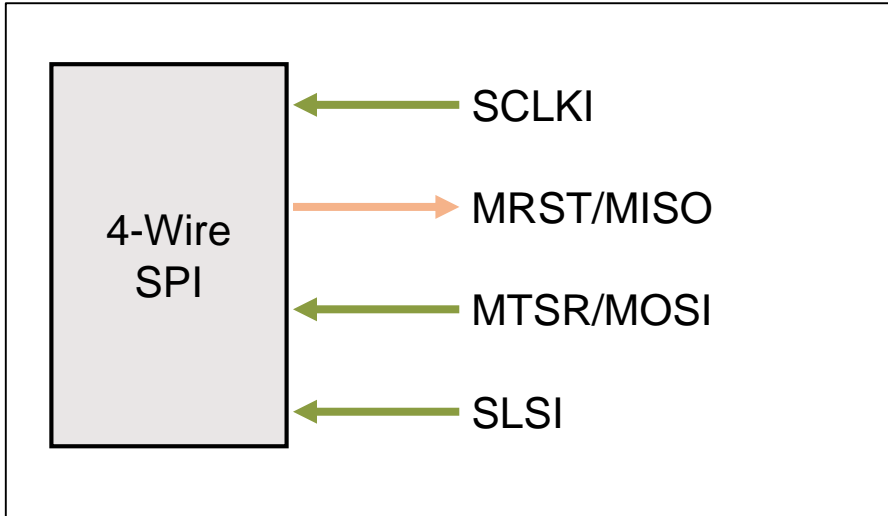# Application example
SPI master
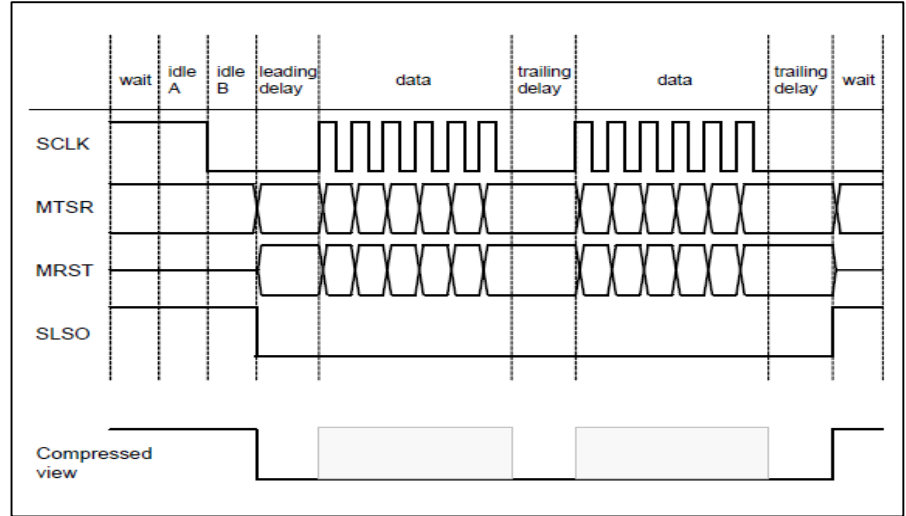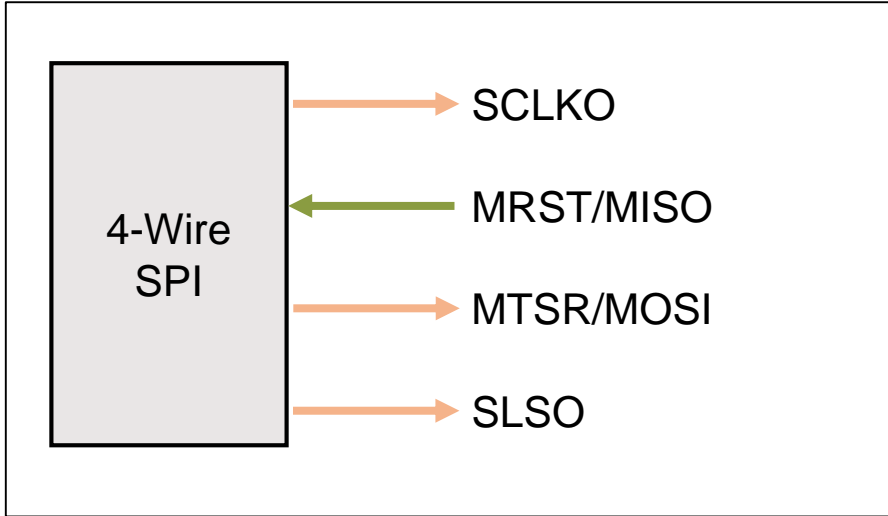
Overview

› Typical 4-wire SPI Master communication

› Support for Full-duplex, Half-duplex and Simplex modes

Advantages

› Full configuration of Idle, Leading and Trailing delays

› Flexible timing control allows to program the duty cycle and the sampling point properties of the serial clock

Application Example
SPI slave

Overview

› Typical 4-wire SPI Slave communication

› Support for Full-duplex, Half-duplex and Simplex modes

Advantages

› Easy configuration with shift clock phase and polarity

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Do you have a question about this document?
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Document reference
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