Clocking
Clocking System

AURIX™ TC3xx Microcontroller Training
V1.0 2020-09

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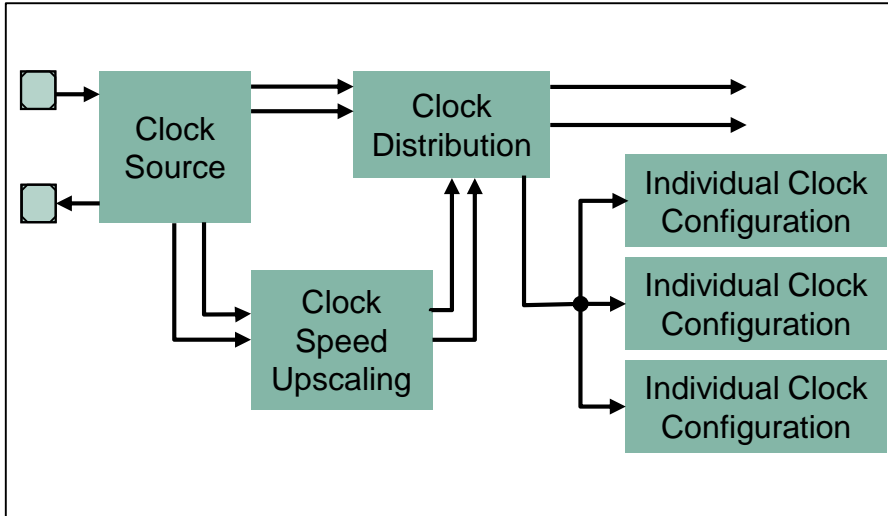
Highlights

› The Clocking System comprises various building blocks, which handle clock generation, upscaling and distribution to all modules

› In AURIX™ TC3xx, external clock input is also supported (e.g. external EDSADC modulator)

Key Features
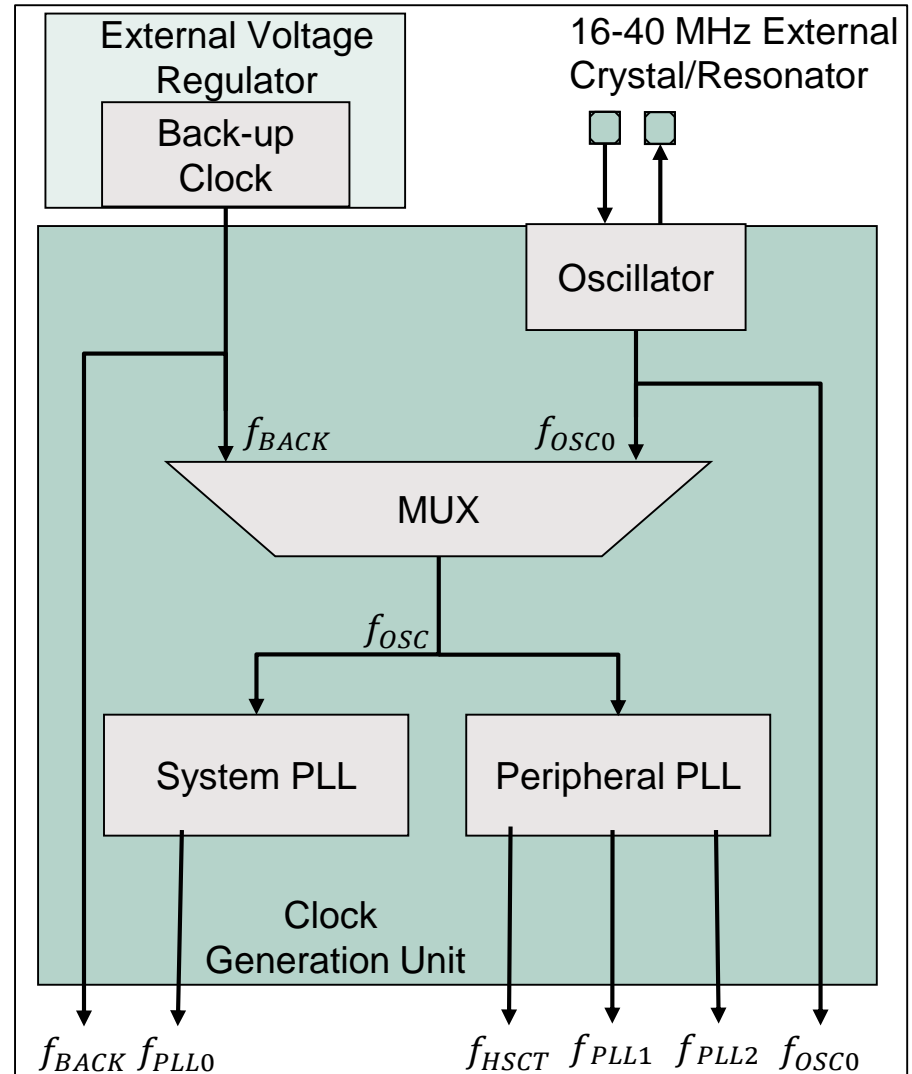
Clock speed upscaling

Clock distribution

Customer Benefits

› Flexible clock configuration according to application needs

› Increased performance and optimized power consumption
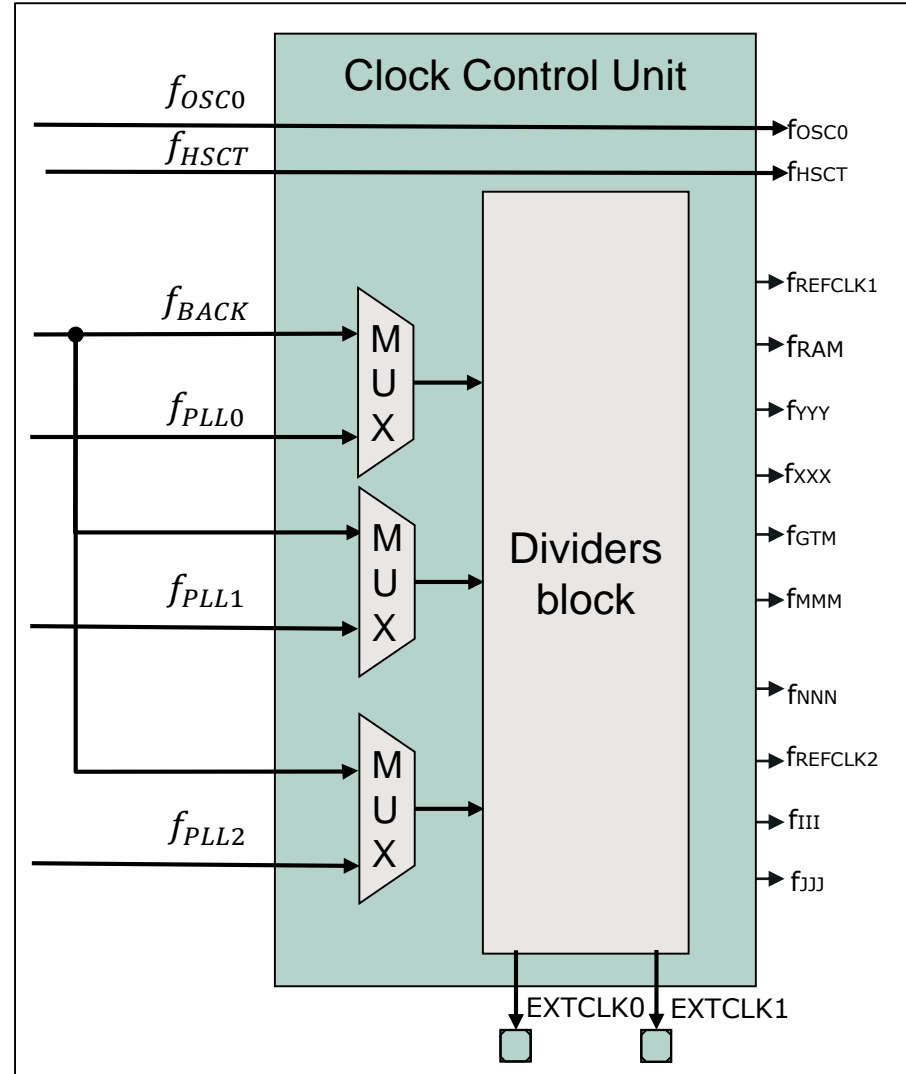
Clocking
Clock Speed Upscaling

› Aside from the pure clock generation options, there are several support functions which aim to enable an easier and more convenient control

› Generally, the CPU operating speed is about 10 times higher than the speed of the crystal used as clock source

› Therefore 2 Phase Lock Loops (PLLs) are provided for upscaling the clock frequency

› The role of the PLL is to convert a low-frequency external clock signal into a high-speed internal clock in order to maximize the performance

› The PLLs from AURIX™ also have fail-safe logic that detects degenerated external clock behaviors such as abnormal frequency deviations or total loss of the external clock

› In these cases, emergency actions can be defined and implemented

External Voltage Regulator	16-40 MHz External Crystal/Resonator
Back-up Clock	

Oscillator

f_{BACK} f_{OSC0}

MUX

f_{OSC}

System PLL Peripheral PLL

Clock Generation Unit

f_{BACK} f_{PLL0} f_{HSCT} f_{PLL1} f_{PLL2} f_{OSC0}

Clocking
Clock distribution

› Based on the clock source and the clock speed upscaling, different clocks are defined and, furthermore, they need to be distributed through the system to the single peripherals and CPUs in a way that enables these modules to operate in the best way in terms of performance and power consumption

› For the clock distribution, the system is split into several sub-clock domains where the clock speed could be configured individually (with the intrinsic restrictions established by the internal interfaces)

› The clock distribution is done via the Clock Control Unit (CCU), which receives the clocks created by the 2 PLLs, the back-up clock and the oscillator clock. These clocks are either forwarded directly or divided in order to supply the sub-clock domains

› This approach increases the flexibility of the system by enabling the user to configure the clock individually for the different modules

Clock Control Unit

f_{OSC0} → f_{OSC0}
f_{HSCT} → f_{HSCT}

f_{BACK}

f_{PLL0}

f_{PLL1}

f_{PLL2}

MUX

Dividers block

→ $f_{REFCLK1}$
→ f_{RAM}
→ f_{YYY}
→ f_{XXX}
→ f_{GTM}
→ f_{MMM}
→ f_{NNN}
→ $f_{REFCLK2}$
→ f_{III}
→ f_{JJJ}

EXTCLK0 EXTCLK1

Clocking
System integration

› AURIX™ TC3xx combines different clocking blocks, which allow a very flexible clock generation for the device

› The frequency can be programmed for an optimal ratio between performance and power consumption

› The PLLs, the clock distribution (CCU) and clock generation unit (CGU) are connected to the System Control Unit (SCU). This enables the monitoring of the frequencies and ensuring that the proper safety measures are taken.
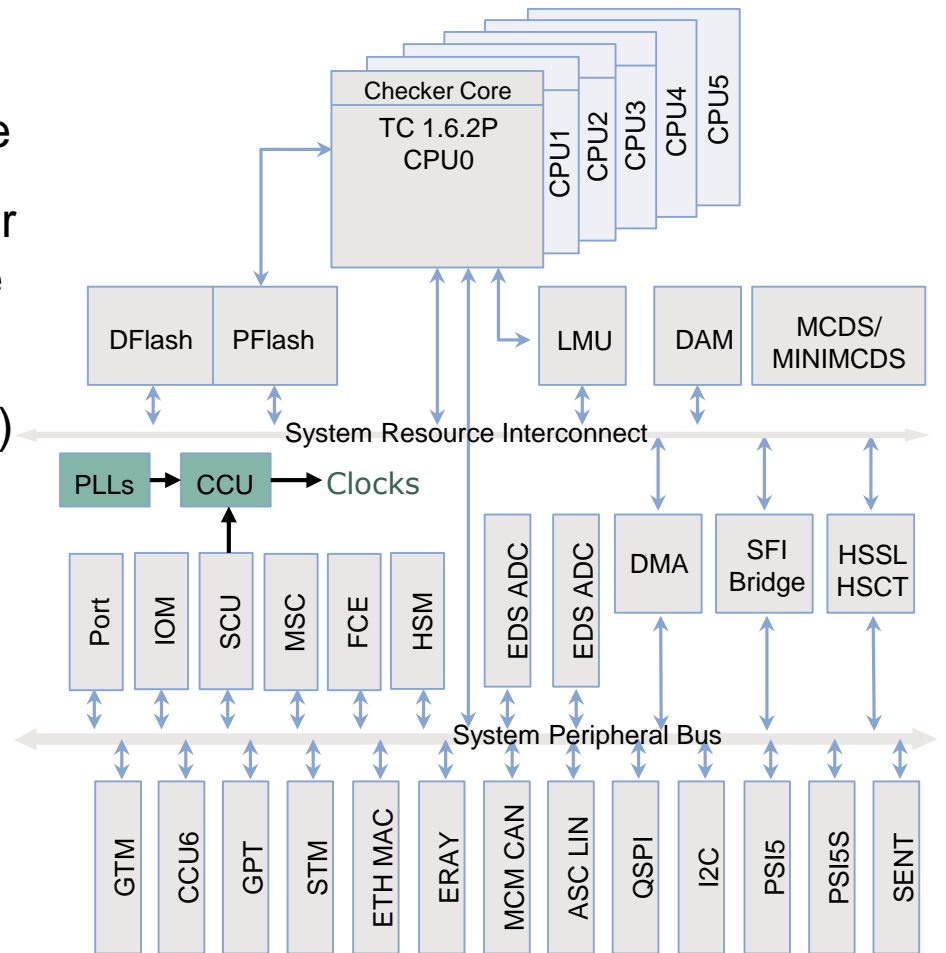
AURIX™ TC39x Block Diagram

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