CPU

Central Processing Unit

AURIX™ TC3xx Microcontroller Training
V1.0 2020-06

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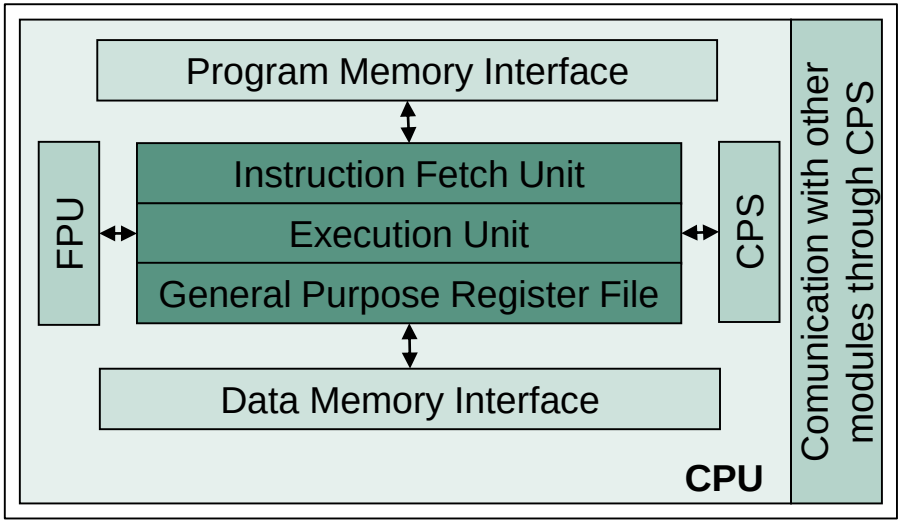


Highlights

› The Central Processing Unit (CPU) comprises of an Instruction Fetch Unit, an Execution Unit, a General Purpose Register File (GPR), a CPU Slave interface (CPS), and Floating Point Unit (FPU).

Key Features

Temporal protection system

Flexible memory protection

Wide range of supported instructions

Customer Benefits

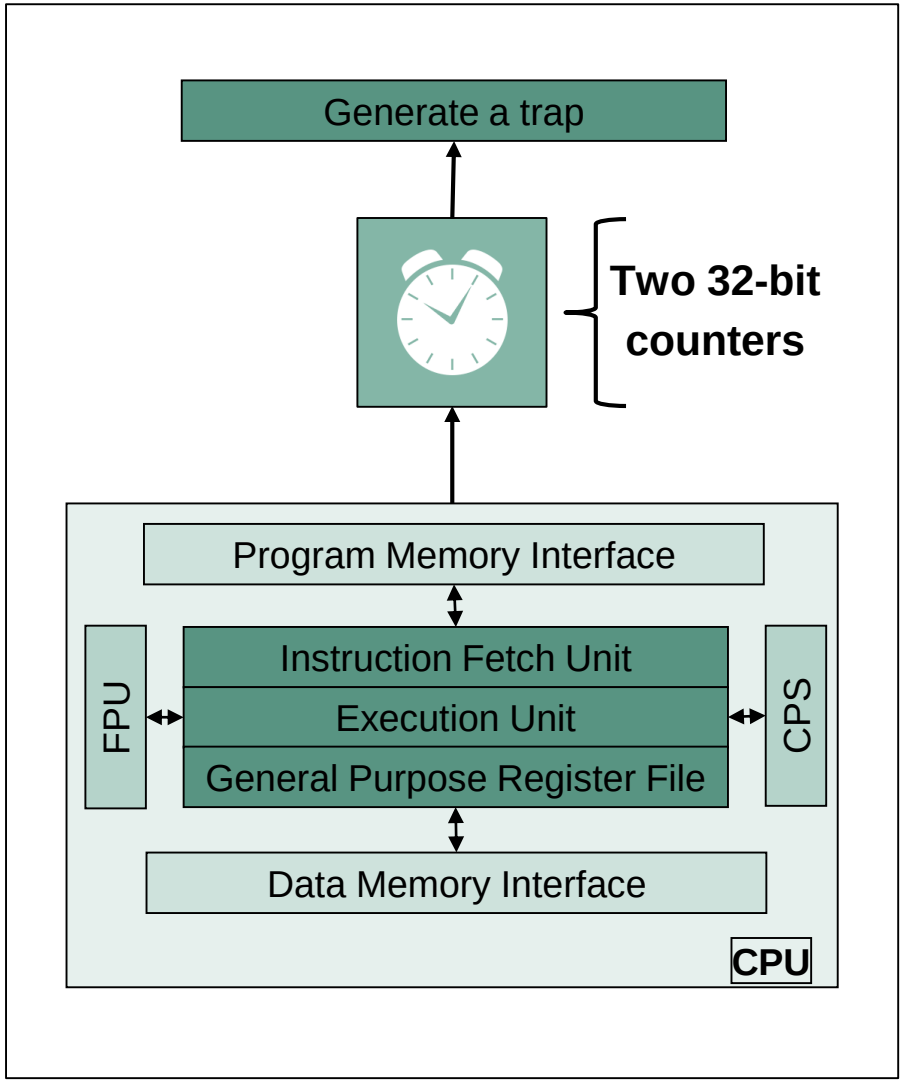
› Time bounded real time operation

› Multiple protection ranges over the memory

› Code optimization (e.g. reduced code size by using 16-bit & 32-bit instructions)

CPU
Temporal protection system

A very common problem of real time systems is given by the tasks with a defined runtime. Overrunning this can lead to overall program failures.
Each core has a temporal protection system (TPS) formed out of three 32-bit decrementing counters clocked by the primary clock.
The operating system (OS) loads the expected runtime at task‘s start and a trap is generated when the counter reaches 0. Generating a trap, and not an interrupt, protects the system in case the task is allowed to disable interrupts for periods of time.
Based on the counters‘ values (together with the time-out flags), it is ensured that the real time application is time bounded.



CPU
Flexible memory protection

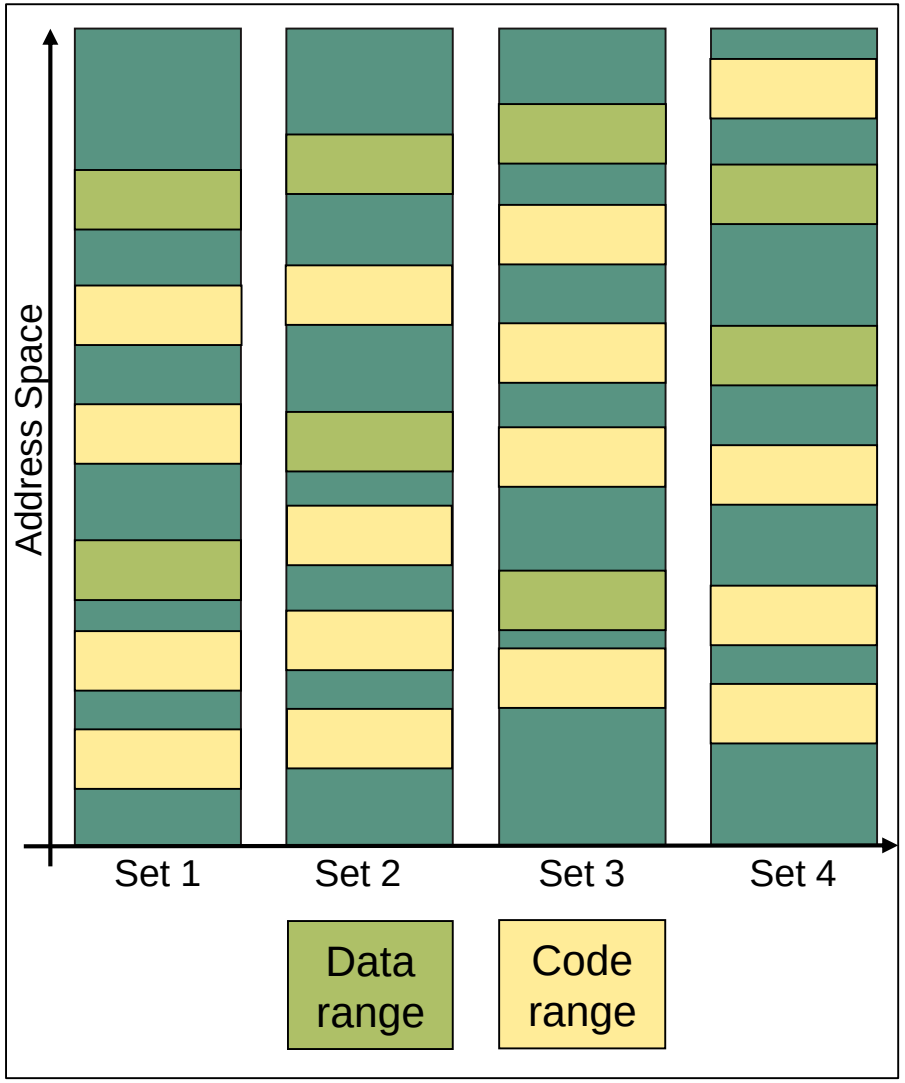
For each task of the real time system, memory resouces are defined. If these resources are outrun, failures appear in the application.

The memory protection stops a program overrunning its assigned region of memory and it is based on access permissions defined by address ranges.

Data access permissions are defined by any combination of write enable and read enable. Fetch access permision is based on access enable rights.

Fast permission switching is based on 6 protection sets with up to 18 defined data ranges and up to 10 defined code ranges.

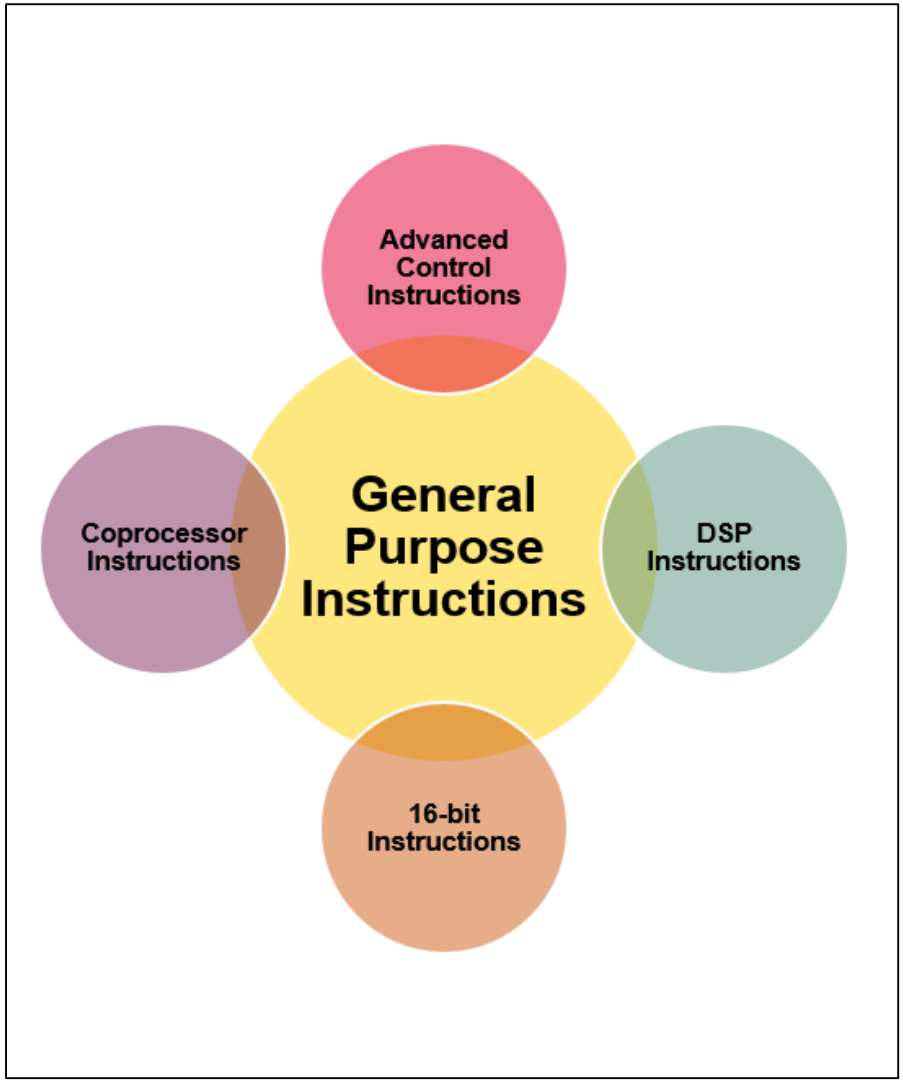
The range to set asignment is flexible, which enables setting the right memory protection for the application at hand.



CPU
Wide range of supported instructions

This very rich instruction set covers 16-bit and 32-bit format instructions, which can be freely mixed in the instruction stream, reducing code size and optimizing the application. The instruction set supports a number of data types including bytes, signed and unsigned integers, single precision floating-point and 16- and 32-bit signed fractions.

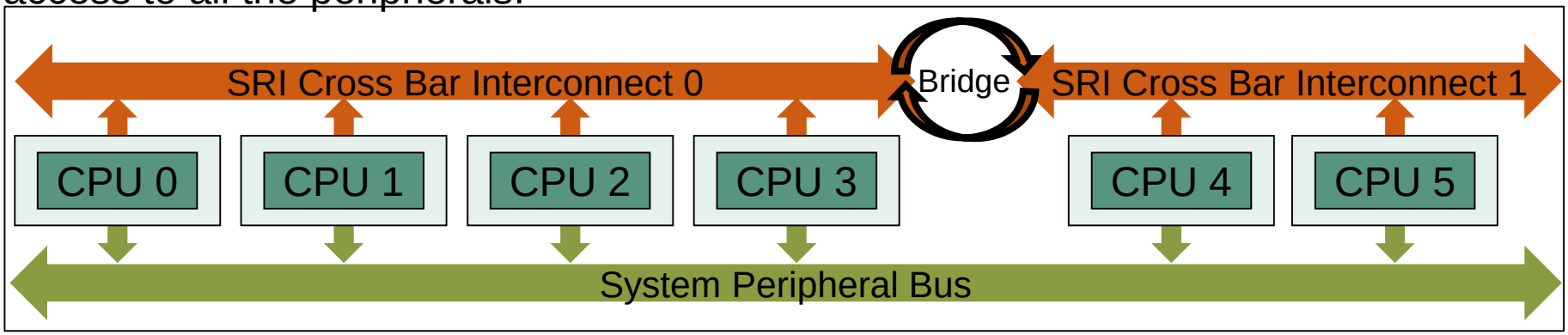
TriCore™ TC1.6.2P Instruction Set	
General Purpose Instr.	Arithmetic, Logic Address Arithmetic & Comparison, Load/Store, Context Switch
Advanced Control Instr.	Bit-field, Bit-logical, Min/Max Comparison, Branch
Coprocessor Instr.	Floating Point
16-bit Subset	Load/Store, Arithmetic, Branch
Digital Signal Processor (DSP) Instr.	MAC, Saturated Math, DSP Addressing Modes



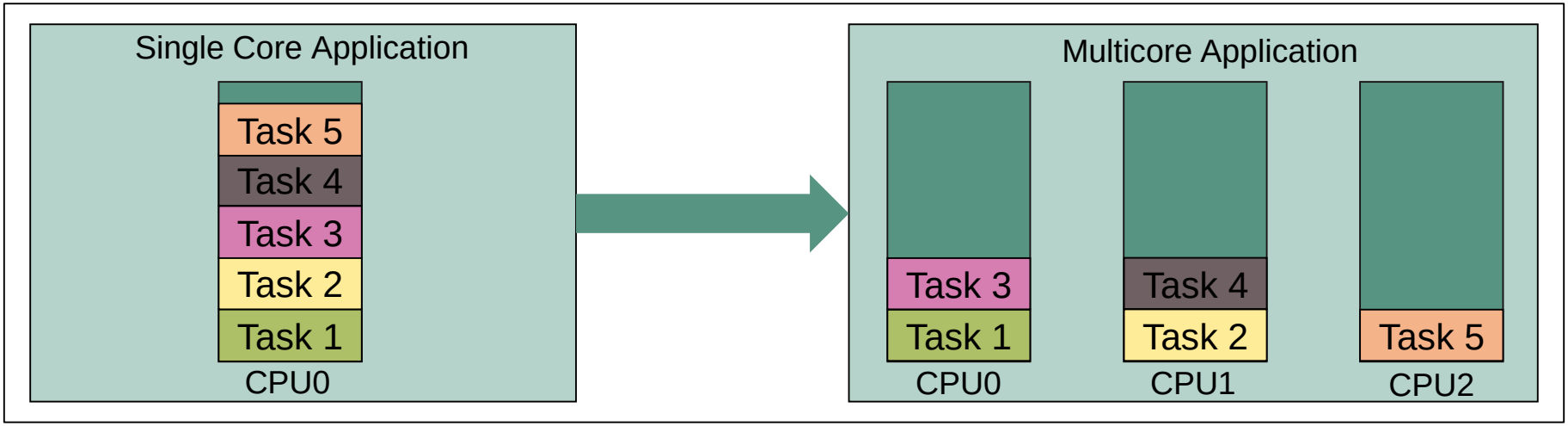
CPU
System Integration

The AURIX™ TC3xx 32-bit microcontroller family contains a wide range of safety oriented devices varying from single-core to hexa-core versions.

One of the most important features of the family is the "lockstep" capability. A core operating in Lockstep mode consists of a master and checker core. The checker core executes the same instructions as the master core, but it is two clock cycles out of phase. In case the outcome of a checker core is different from the master, an alarm is generated.
The cores 0 to 3 are connected to SRI Cross Bar Interconnect 0 (SRI0), while cores 4 and 5 are connected to SRI Cross Bar Interconnect 1 (SRI1). The two cross bars are connected via a bridge. This ensures the fast exchange of data between the cores. Moreover, the CPUs are connected to the System Peripheral Bus, which grant them access to all the peripherals.



Application Example
Multicore application



Overview

Issue: Real-time applications running multiple tasks have the issue of overloading the CPU.

Solution: Switching to a multicore system, where tasks are divided over multiple cores. In the case of tasks depending on each other, the needed communication and scheduling will slightly reduce the performance.

Advantages

- Avoid CPU overload
- Improvement of overall system‘s performance
- Clear division of tasks over the whole system (moving from „one-man show“ to „team work“)

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