CCU_Clock_1
for KIT_AURIX_TC334_LK
Clock configuration via CCU

AURIX™ TC3xx Microcontroller Training
V1.0.0

Scope of work

The clock system is configured based on a PLL frequency of 200 MHz and the clock signal is provided at an external port pin.

The Clock Control Unit (CCU) is used to configure the PLL clock. This clock signal is routed to an external clock output pin, which can be observed with an oscilloscope.

Introduction

- The Clock Control Unit (CCU) controls the clock system and contains different blocks:
  - Basic clock generation
  - Clock speed upscaling
  - Clock distribution
  - Individual clock configuration
- The Clock Generation Unit (CGU) is part of the CCU and allows a flexible clock generation
- Phase Lock Loops (PLLs) are provided for upscaling the clock frequency from an internal or external oscillator
- The System Peripheral Bus (SPB) is used to enable the Fractional Divider (FDR) to divide the source clock

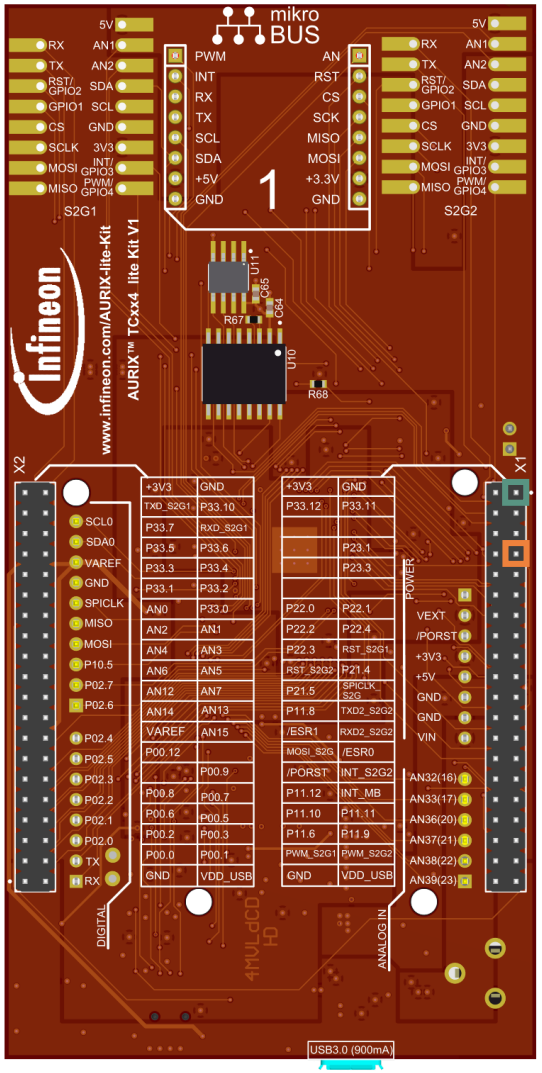
Note: For backward compatibility, some of the registers and functions have the prefix „SCU“ (System Control Unit). In AURIX™ TC2xx, the clocking system was a part of the System Control Unit.

Hardware setup

This code example has been developed for the board KIT_A2G_TC334_LITE.

An oscilloscope is needed to observe the clock at the pin P23.1. Connect the clock and the ground to the oscilloscope.

		X1		
	+3V3	2	1	GND
	P33.12	4	3	P33.11
	N.C.	6	5	N.C.
	N.C.	8	7	P23.1
	N.C.	10	9	N.C.
	N.C.	12	11	N.C.
	P22.0	14	13	P22.1
	P22.2	16	15	P22.4
	P22.3	18	17	P21.2 - RST_S2G1
RST_S2G2 -	P21.3	20	19	P21.4
	P21.5	22	21	P20.11 - SPICLK_S2G
	P11.8	24	23	P20.0 - TXD2_S2G2
	/ESR1	26	25	P20.3 - RXD2_S2G2
MOSI_S2G -	P20.14	28	27	/ESR0
Reset -	/PORST	30	29	P15.5 - INT_S2G2
	P11.12	32	31	P15.4 - INT_MB
	P11.10	34	33	P11.11
	P11.6	36	35	P11.9
PWM_S2G1 -	P11.2	38	37	P11.3 - PWM_S2G2
	GND	40	39	VDD_USB



Implementation

Configuring Clock Control Unit

Configuration of the Clock Control Unit (CCU) is done once in the setup phase by calling the initialization function ***initCcuClock()***, which contains the following steps:

- Create an instance of the ***IfxScuCcu_Config*** structure which contains the CCU configuration
- Initialize the configuration by calling the iLLD function ***IfxScuCcu_initConfig()***
- Set the PLL dividers (N, P, K2) to get the desired PLL frequency (see page 6) (the desired frequency is 200 MHz for this example)
- Initialize the CCU with the iLLD function ***IfxScuCcu_init()***
- Set SPB frequency to the desired value by calling the function ***IfxScuCcu_setSpbFrequency()*** (SPB frequency is 100 MHz for this example)

The ***initCcuClock()*** function is contained in the ***CCU_Clock.h***, while the other functions are part of the iLLD header ***IfxScuCcu.h***.

Implementation

PLL divider calculation example

The PLL frequency (f_{pll0}) is defined according to the following formula:

$$f_{pll0} = \frac{f_{osc} * N}{K2 * P}$$

where the oscillator's frequency (f_{OSC}) is 20 MHz (dependent on hardware).

In this example f_{pll0} = 20 MHz, therefore $\frac{N}{K2 * P} = 20$. To obtain this value, N should be set to 20, P to 1 and K2 to 2 (P = 1 and K2 = 2 are the defaults values).

Note: For selecting appropriate values for the dividers, please consult the User Manual.

Implementation

Configuring the Clock output

Configuration of the clock output is done once in the setup phase by calling the initialization function ***configOutputCcuClock()***, which contains the following steps:

- Call the iLLD function ***IfxScuWdt_clearSafetyEndinitInline()*** to disable the Safety Endinit protection in order to modify the SCU register
- Set ***SCU_CCUCON0.B.CLKSEL*** to 0x1 to select the clock source
- Set ***SCU_EXTCON.B.EN0*** and ***SCU_EXTCON.B.SEL0*** to enable and select output frequency (f_{OUT}) as external source (***SCU_EXTCON.B.EN0*** = 0x1, ***SCU_EXTCON.B.SEL0*** = 0x0)
- Set ***SCU_FDR.B.STEP*** to the desired reload value (see page 9) and ***SCU_FDR.B.DM*** to choose the normal divider mode
- Call the iLLD function ***IfxScuWdt_setSafetyEndinitInline()*** to re-enable the Safety Endinit protection

The functions ***IfxScuWdt_clearSafetyEndinitInline()*** and ***IfxScuWdt_setSafetyEndinitInline()*** are contained in iLLD header ***IfxScuWdt.h***.

Implementation

Configuring the port pin

Configuration of the port pin is done as well in the function ***configOutputCcuClock()*** with the following steps:

- Call the iLLD function ***IfxPort_setPinMode()*** with ***IfxPort_Mode_outputPushPullAlt6*** as parameter to select CCU external clock as output
- Set pin pad driver to increase pin‘s speed by calling the iLLD function ***IfxPort_setPinPadDriver()*** and setting ***IfxPort_PadDriver_cmosAutomotiveSpeed1*** as parameter

The functions ***IfxPort_setPinMode()*** and ***IfxPort_setPinPadDriver()*** are contained in iLLD header ***IfxPort.h***.

Implementation

Step Value calculation example

The Step Value in normal divider mode is defined according to the following formula:

$$f_{OUT} = \frac{f_{SPB} * \frac{1}{n}}{\mathbf{2}}, \text{with n} = 1024 - Step$$

$$\text{Therefore}, Step = 1024 - \frac{f_{SPB}}{\mathbf{2} * f_{OUT}}$$

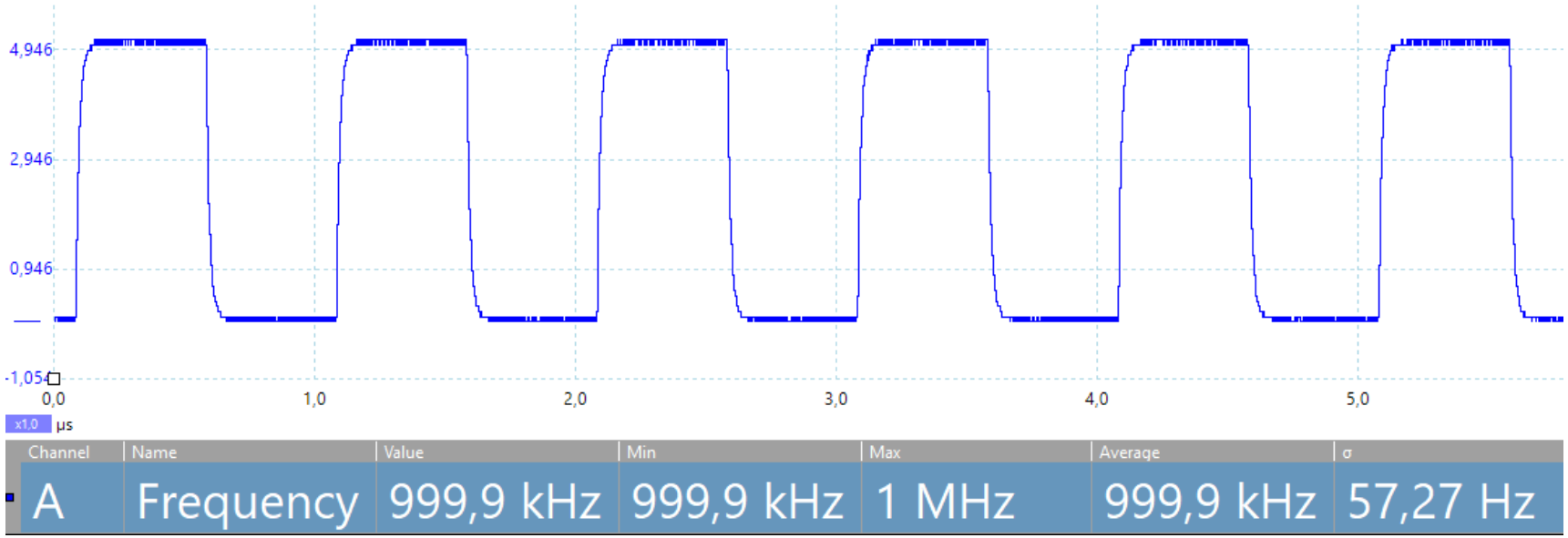
In this example, the desired external frequency value (f_{OUT}) is 1 MHz, and f_{SPB} is 100 MHz.
After calculation, the Step Value is 974 (0x3CE).

Run and Test

After code compilation and flashing the device, perform the following steps:

› Connect the oscilloscope to the board via port pin P23.1 and ground

› Observe the desired clock on the oscilloscope’s screen



References

- AURIX™ Development Studio is available online:
- https://www.infineon.com/aurixdevelopmentstudio
- Use the *„Import...“* function to get access to more code examples.

- More code examples can be found on the GIT repository:
- https://github.com/Infineon/AURIX_code_examples

- For additional trainings, visit our webpage:
- https://www.infineon.com/aurix-expert-training

- For questions and support, use the AURIX™ Forum:
- https://www.infineonforums.com/forums/13-Aurix-Forum

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