Customer Training Workshop

Traveo™ II Automotive Cluster 2D Power Supply and Monitoring

Q4 2020

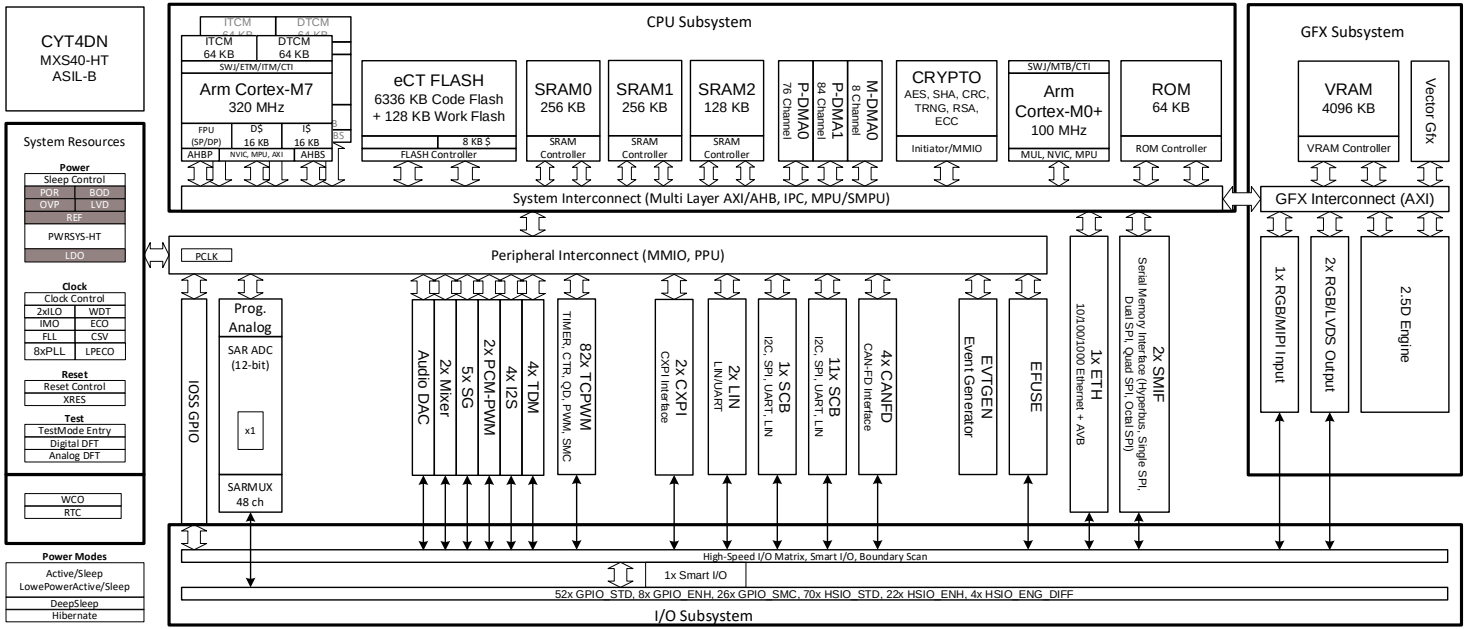
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster	CYT3DL	Up to 4160 KB
Traveo™ II Automotive Cluster	CYT4DN	Up to 6336 KB

Introduction

› Power supply monitoring functions are in System Resources



Hint Bar

Review TRM section 16.2 for additional details

Power-on reset (POR)

Brownout detection (BOD)

Over-voltage detection (OVD)

Low-voltage detection (LVD)

Low drop-out regulator (LDO)

Power Supply Overview

- 2.7–5.5-V power supply range
- Core regulators for High Current, Active, and DeepSleep modes

Digital power supply

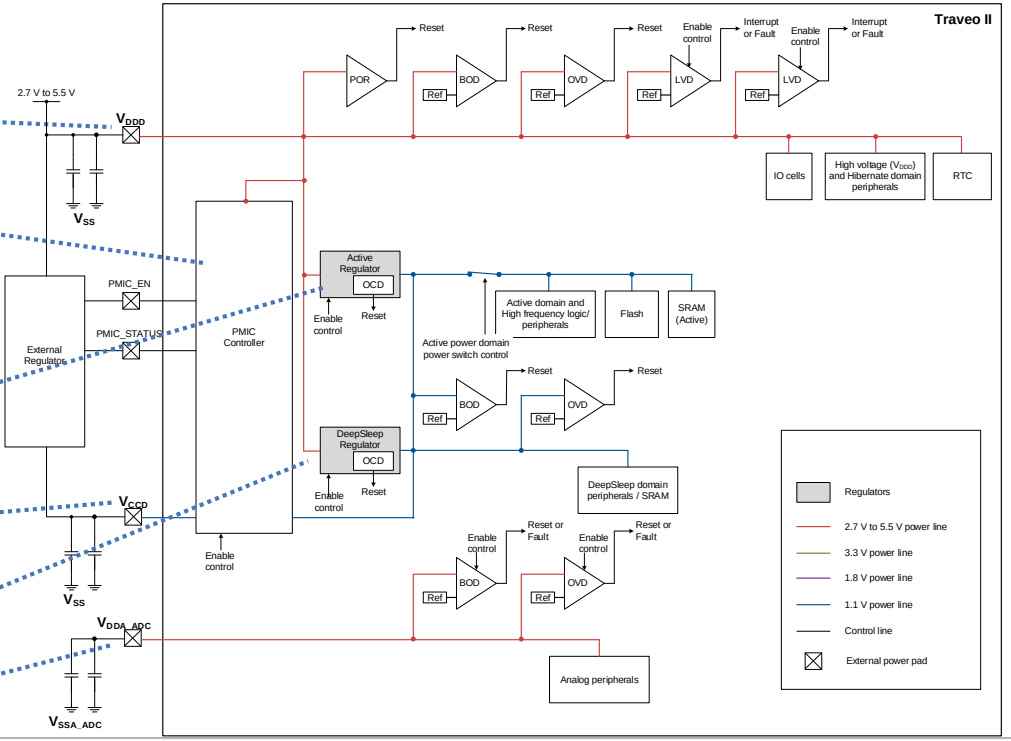
External high-current regulator controller with load current up to 600 mA

Internal logic supply for device startup (boot process) and for applications with load current up to 300 mA

Core power supply

Internal logic power supply for DeepSleep mode

Analog power supply



Hint Bar

Review TRM section 16.2 for additional details

V_{DDD}/V_{SS}: Digital power supply/ ground

V_{DDA_ADC}/V_{SSA_ADC}: Analog power supply/ ground

V_{CCD}/V_{SS}: Internal core supply/ ground

Power Pins and Rails

Power/ground pins and voltage range

Supply Pin	Ground Pin	Power Supply Voltage Range	Description
V_{DDD}	V_{SS} or V_{SSD}	2.7 V to 5.5 V	Digital and GPIO supply
V_{CCD}	V_{SS} or V_{SSD}	1.09 V to 1.21 V	Core supply
V_{DDIO_SMIF}	V_{SS}	1.7 V to 2.0 V	HSIO_ENH I/O supply for 1.8-V SMIF
$V_{DDIO\_SMIF\_HV}$	V_{SS}	3.0 V to 3.6 V	HSIO_STD I/O supply for 3.3-V SMIF
V_{DDIO_HSIO}	V_{SS} or V_{SSIO_HSIO}	3.0 V to 3.6 V	HSIO_STD I/O supply
V_{DDIO_SMC}	V_{SS} or V_{SSIO_SMC}	2.7 V to 5.5 V	SMC I/O supply
V_{DDIO_GPIO}	V_{SS} or V_{SSIO_GPIO}	2.7 V to 5.5 V	GPIO supply
V_{DDHA_FPD0}	V_{SSA_FPD0}	3.0 V to 3.6 V	FPD-Link0 line drivers supply
V_{DDA_FPD0}	V_{SSA_FPD0}	1.09 V to 1.21 V	FPD-Link0 core supply
V_{DDPLL_FPD0}	V_{SSA_FPD0}	1.09 V to 1.21 V	FPD-Link0 PLL supply
V_{DDHA_FPD1}	V_{SSA_FPD1}	3.0 V to 3.6V	FPD-Link1 line drivers supply
V_{DDA_FPD1}	V_{SSA_FPD1}	1.09 V to 1.21 V	FPD-Link1 core supply
V_{DDPLL_FPD1}	V_{SSA_FPD1}	1.09 V to 1.21 V	FPD-Link1 PLL supply
V_{DDA_MIPI}	V_{SSA_MIPI}	1.09 V to 1.21 V	D-PHY supply
V_{DDA_ADC}	V_{SSA_ADC}	2.7 V to 5.5 V	Analog supply voltage
V_{DDA_DAC}	V_{SSA_DAC}	3.0 V to 3.6 V	Audio DAC supply

Hint Bar

Review TRM section 16.2.2 for additional details

Power Supply

- Power supply sources
  - Multiple analog supply rails and V_{DDIO} rails exist independent of V_{DDD} and V_{CCD}

- Power sequencing requirements
  - 1.15-V nominal supplies all need to be shorted, at the same level, and with the same presence
- Advantage
  - Less effort and cost because no external power sequencing control is required for applications with load current up to 300 mA

Hint Bar

Review the datasheet

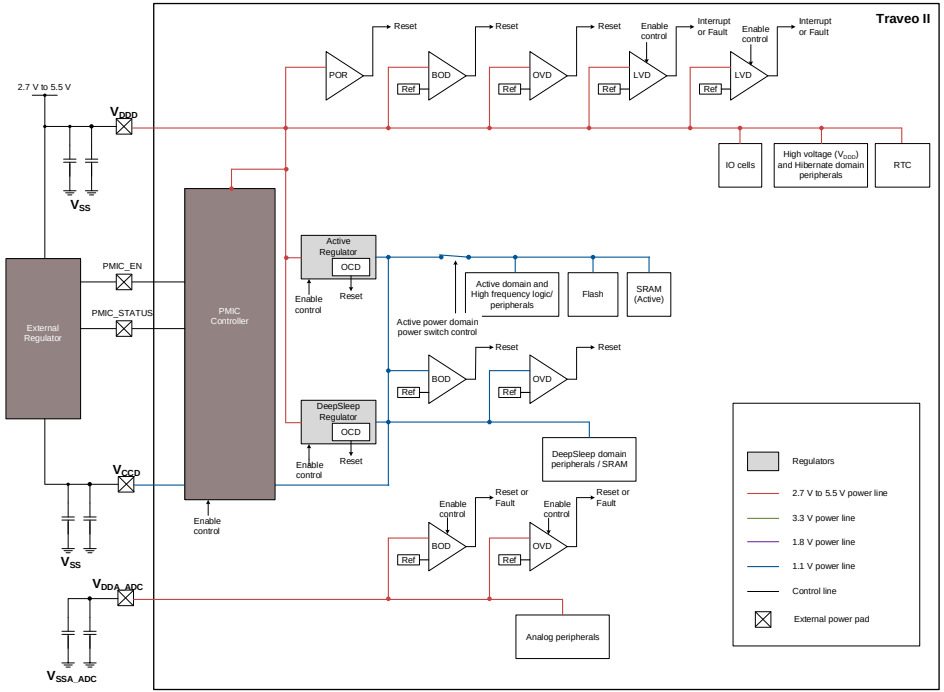
Recommended Operating Conditions

12-Bit SAR ADC DC Specifications when using ADC units

Review TRM sections 16.2.3 and 16.2.4 for additional details

Regulator Selection

- PMIC controller selection
  - Device starts up with Active regulator, which supports up to 300 mA supply current
  - Switches to PMIC controller if supply current of up to 600 mA is required

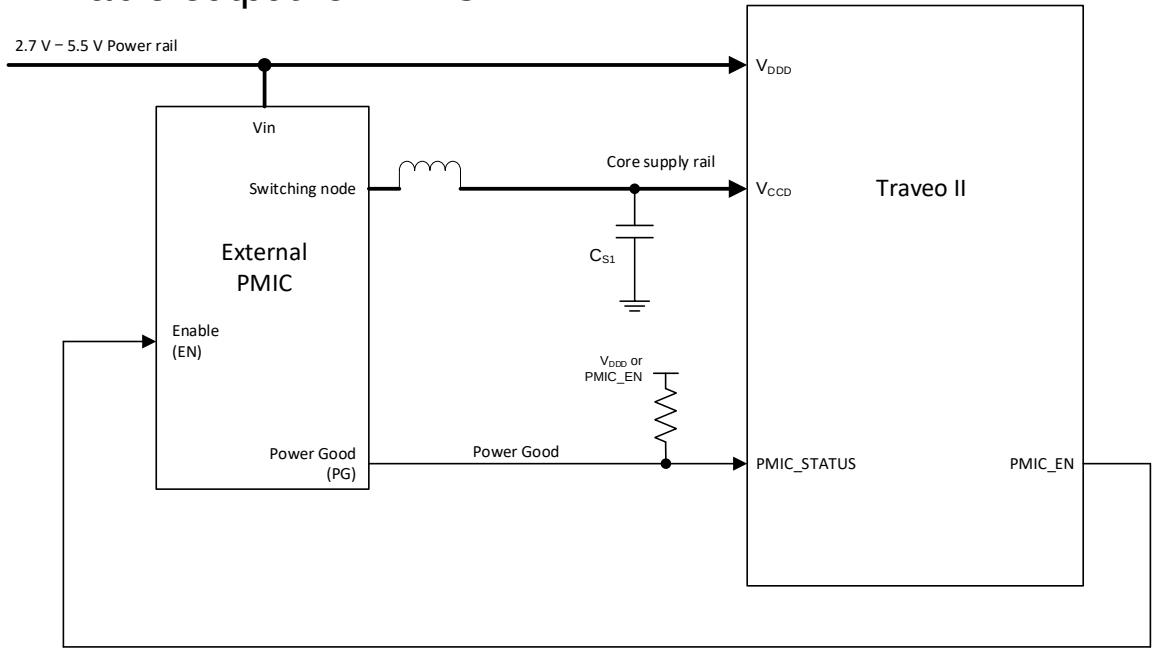


Hint Bar

Review datasheet and TRM section 16.2.5 for additional details

External PMIC Configuration (Hardware)

- PMIC controller pins
  - PMIC_STATUS: Power Good input from PMIC
  - PMIC_EN: Enable output for PMIC



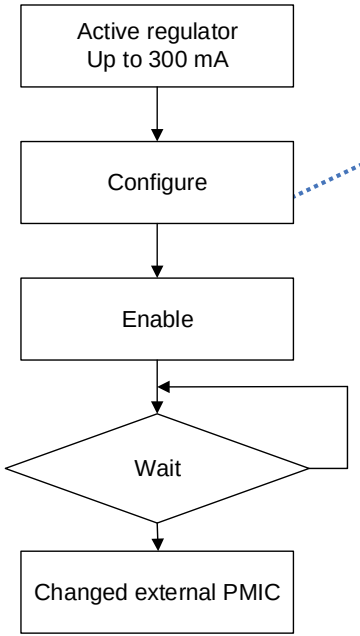
Hint Bar

Review datasheet and TRM section 16.2.5 for additional details

Recommended PMICs: Cypress S6BP501A and Rohm BD9S200MUF-C

External PMIC Configuration (Software)

- Changing from active regulator to external PMIC
  - Setup flow



Call ConfigureRegulator API:

- PWR_PMIC_CTL.PMIC_STATUS_INEN = 1 to enable the input path for PMIC status
- PWR_PMIC_CTL.PMIC_STATUS_POLARITY to the setting that indicates an error condition (depending on the polarity of the PMIC status output)
- PWR_PMIC_CTL.PMIC_CTL_OUTEN = 1 and PWR_PMIC_CTL.PMIC_CTL_POLARITY to the setting that enables the PMIC (depending on polarity of PMIC enable input)
- PWR_PMIC_CTL.PMIC_CONFIGURED = 1

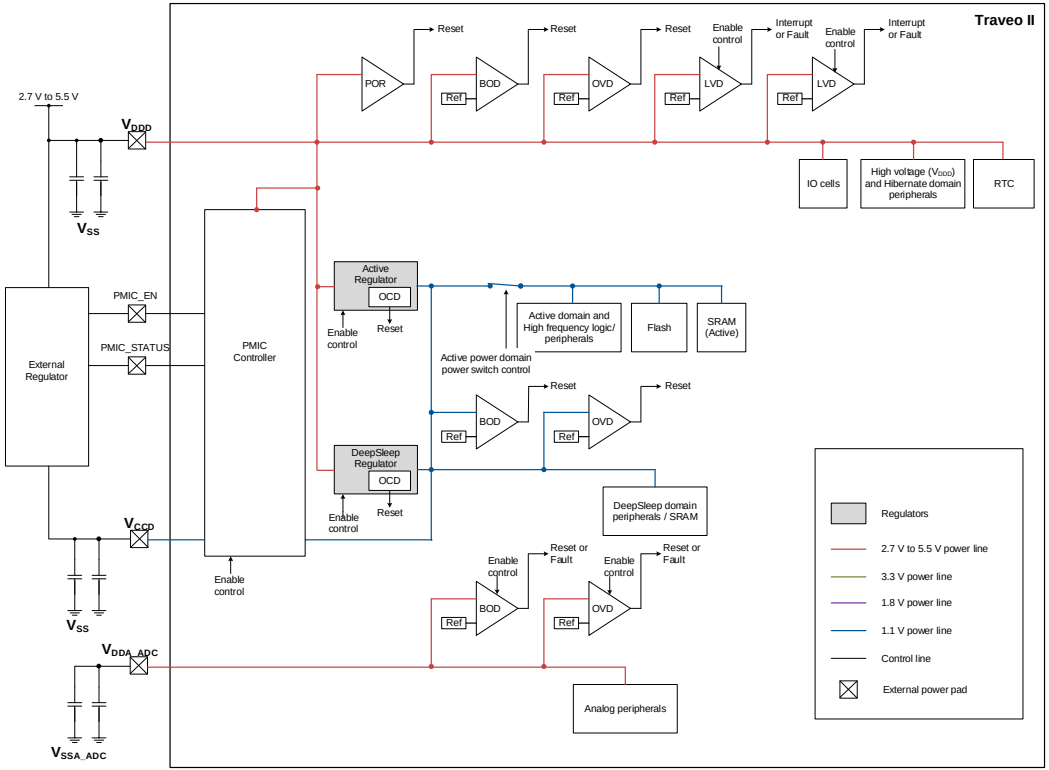
Call SwitchOverRegulators API:

- PWR_PMIC_CTL2.PMIC_EN = 1
- Wait until PWR_PMIC_STATUS.SEQ_BUSY = 0 and PWR_PMIC_STATUS.PMIC_ENABLED = 1

This delay depends strongly on the startup time of the PMIC, based on its status output and the value in PWR_PMIC_CTL.PMIC_STATUS_WAIT

Voltage Monitoring Overview

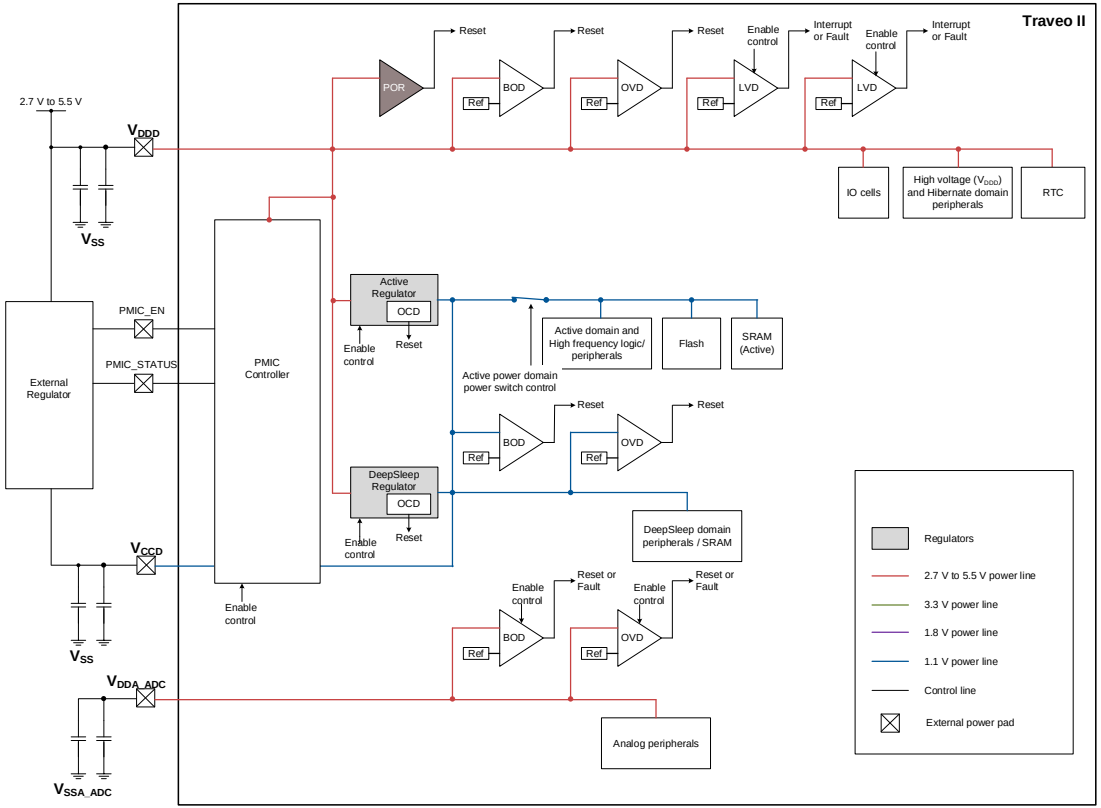
› Supports multiple voltage monitoring features and supply failure protection



Hint Bar

Review datasheet and TRM section 16.3 for additional details

Power-on Reset (POR) Block Diagram

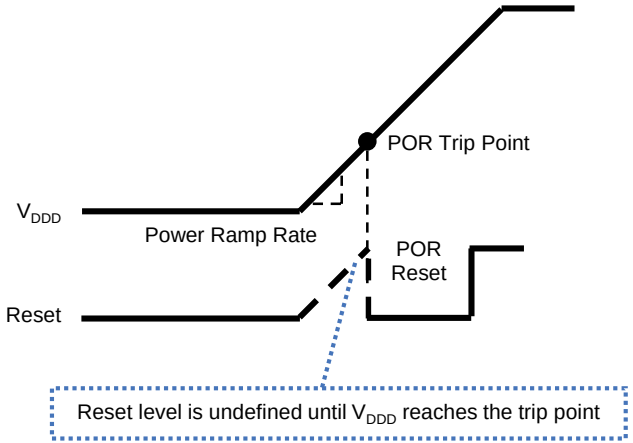


Hint Bar

Review datasheet and TRM section 16.3 for additional details

POR Features

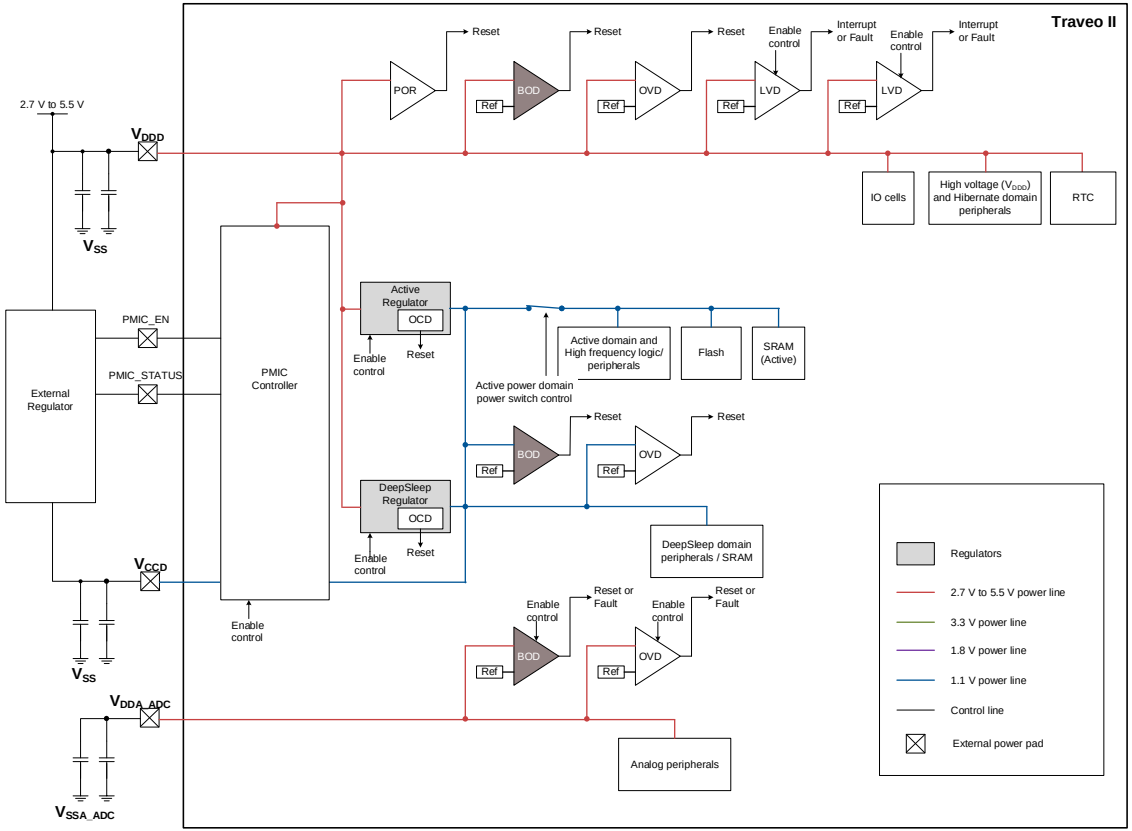
- Initializes the device at power-up
- Always on
  - POR on V_{DDD}
    - Provides a reset pulse during the initial power ramp



Hint Bar

Review datasheet and TRM section 16.3.1 for additional details

Brown-out Detection (BOD) Block Diagram

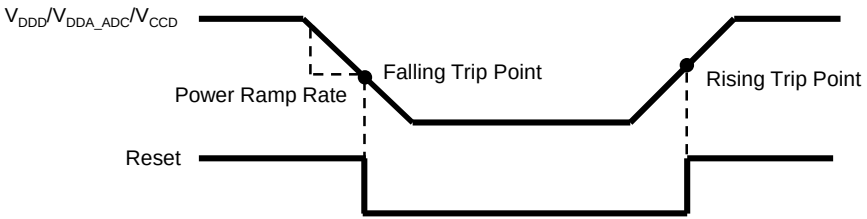


Hint Bar

Review datasheet and TRM section 16.3 for additional details

BOD Features

- Detects supply condition below a threshold and applies a reset to the device
- Always on except in Hibernate and XRES modes
  - BOD on V_{DDD}
    - Generates a reset if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on V_{DDA_ADC}
    - Generates a reset, a fault, or no action[2] (default) if a voltage excursion dips below the falling trip point
    - Supports two trip points: < 2.7 V[1] (default) or < 3.0 V
  - BOD on V_{CCD}
    - Generates a reset if a voltage excursion dips below the falling trip point

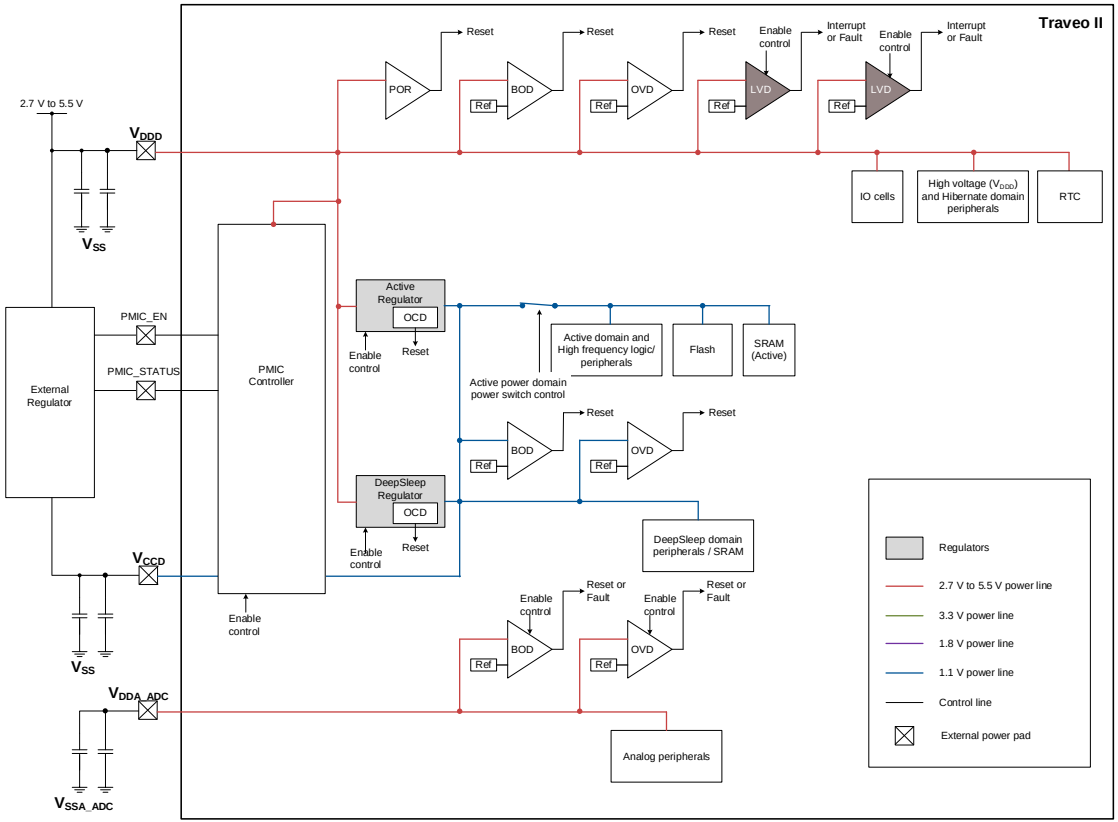


Hint Bar

Review datasheet and TRM section 16.3.2 for additional details

[1] If V_{DDD}/V_{DDA_ADC} falls below 2.7 V (minimum V_{DDD}/V_{DDA_ADC}), the device will operate out of specification. To prevent that, use the 3.0-V trip point
[2] Even if V_{DDA_ADC} is low, the MCU can boot because it does not generate a reset as default

Low-Voltage Detection (LVD) Block Diagram

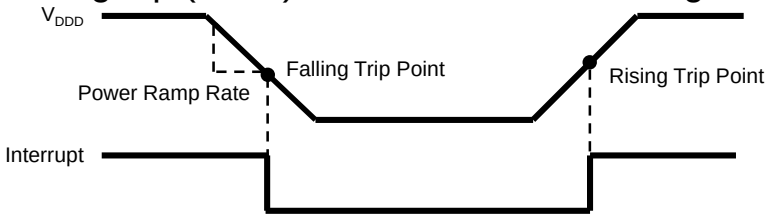


Hint Bar

Review datasheet and TRM section 16.3 for additional details

LVD Features

- Detects the warning voltage level to take preventive measures in the system
- Can be enabled or disabled (default) by software, except in Hibernate and XRES modes
  - LVD on V_{DDD}
    - Generates an interrupt or a fault if a voltage level meets the trip point
    - An interrupt or a fault and trip point are configurable by software
      - Supports up to 26 trip points to monitor between 2.8 V and 5.3 V (0.1-V step)
    - Can be configured as falling (low voltage), rising (high voltage) detection, or both
- Use case for two LVD units
  - LVD1: Use the falling trip point (3.5 V) to detect the low-voltage warning
  - LVD2: Use the rising trip (5.3 V) to detect the over-voltage warning

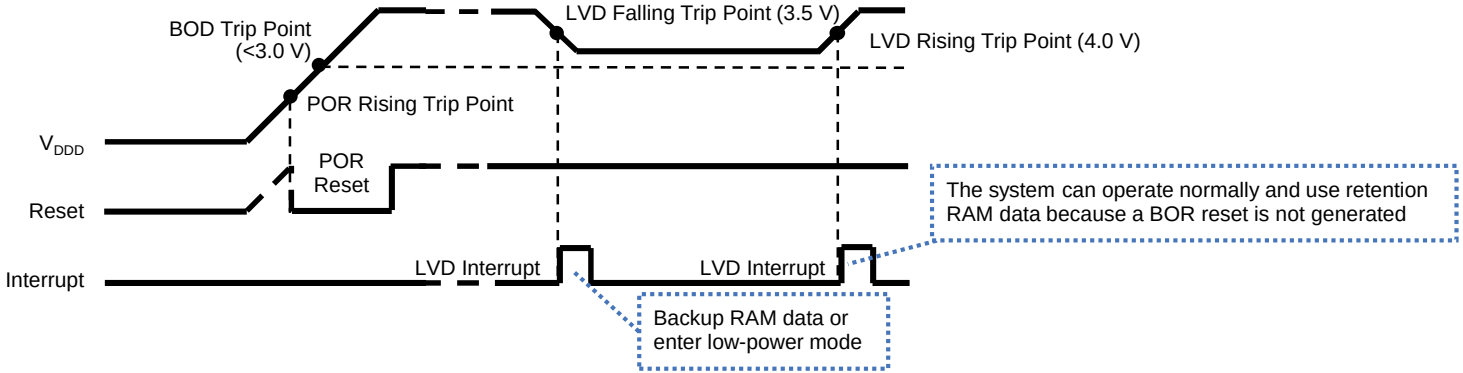


Hint Bar

Review datasheet and TRM section 16.3.4 for additional details

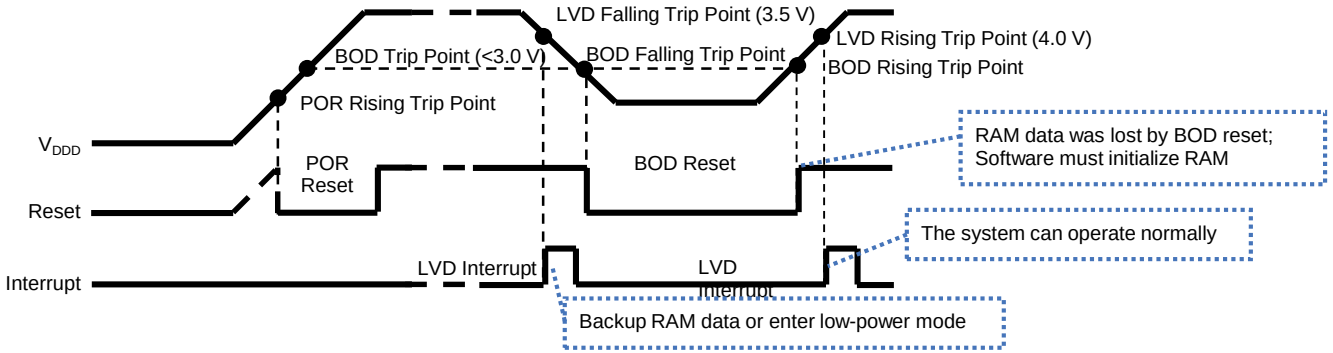
POR, BOD, and LVD Use Cases (1/2)

- Purpose: Judge whether RAM contents have been retained by using voltage monitoring
- Setting and condition
  - MCU operation conditions
    - LVD trip point can be in MCU operation range − RAM retention
      - LVD falling trip point (3.5 V): Warning LVD for safety system operation
      - LVD rising trip point (4.0 V): User program restart trigger
    - BOD reset (<3.0 V) is an asynchronous reset − No RAM retention
- Use Case: For RAM, contents are retained (no BOD reset generation)



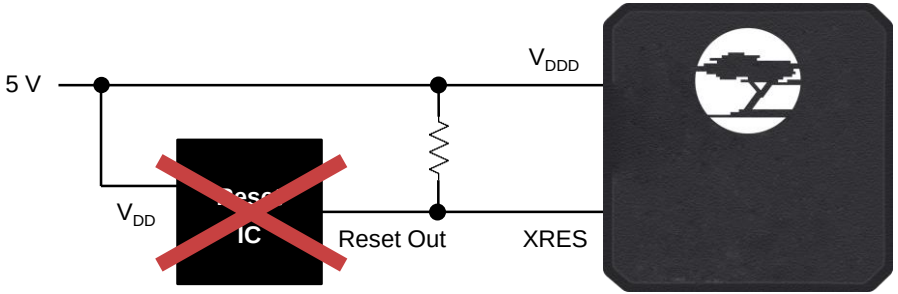
POR, BOD, and LVD Use Cases (2/2)

- Purpose: Judge whether RAM contents have been retained by using voltage monitoring
- Setting and condition
  - MCU operation conditions:
    - LVD trip point can be in MCU operation range − RAM retention
      - LVD falling trip point (3.5 V): Warning LVD for safety system operation
      - LVD rising trip point (4.0 V): User program restart trigger
    - BOD reset (<3.0 V) is an asynchronous reset − No RAM retention
- Use Case: For RAM, contents have not been retained (BOD reset generation)



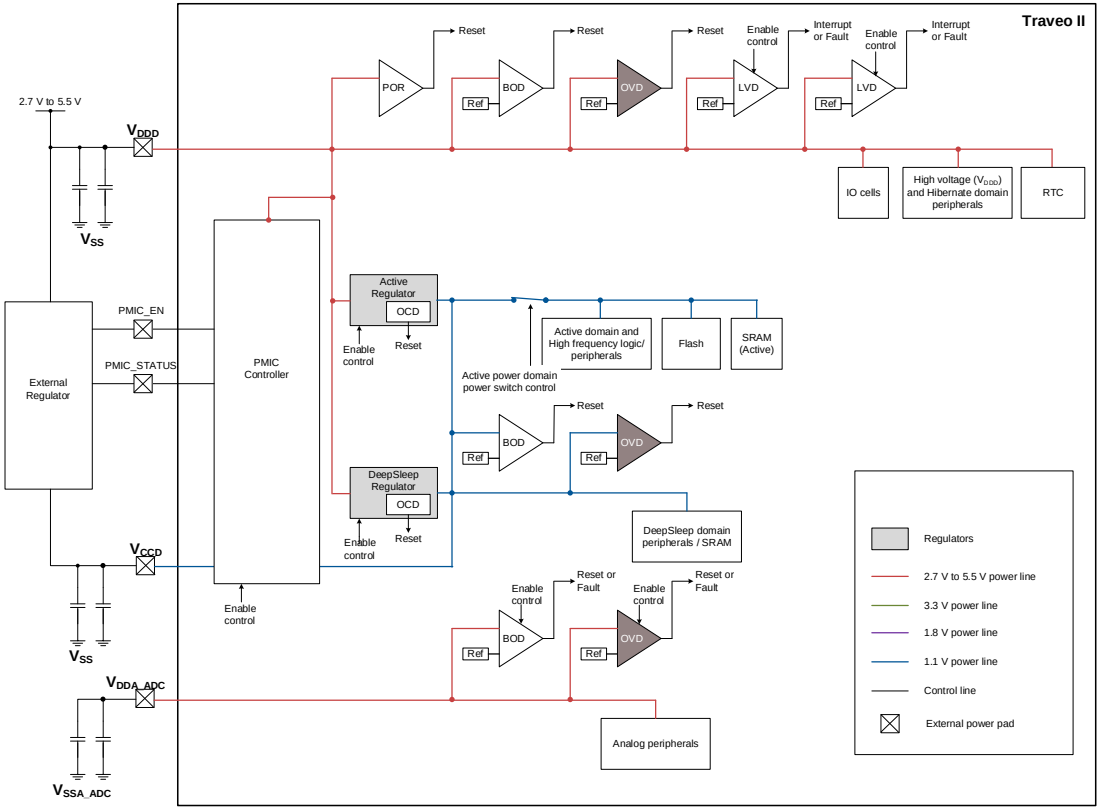
POR, BOD, and LVD Advantage

› Reduced BOM costs for low-cost applications using internal POR, BOD, and LVD[1]



[1] Review TRM and datasheet to confirm if the POR, BOD, and LVD specifications meet the safety requirements of the system

Overvoltage Detection (OVD) Block Diagram

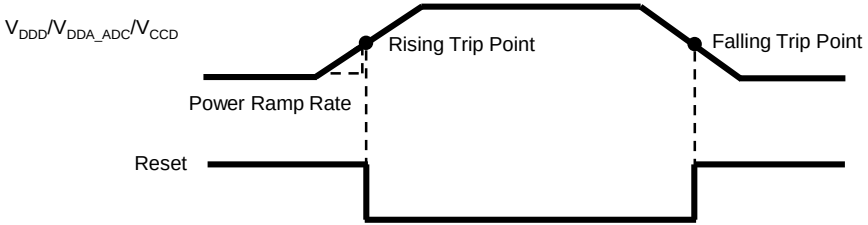


Hint Bar

Review datasheet and TRM section 16.3 for additional details

OVD Features

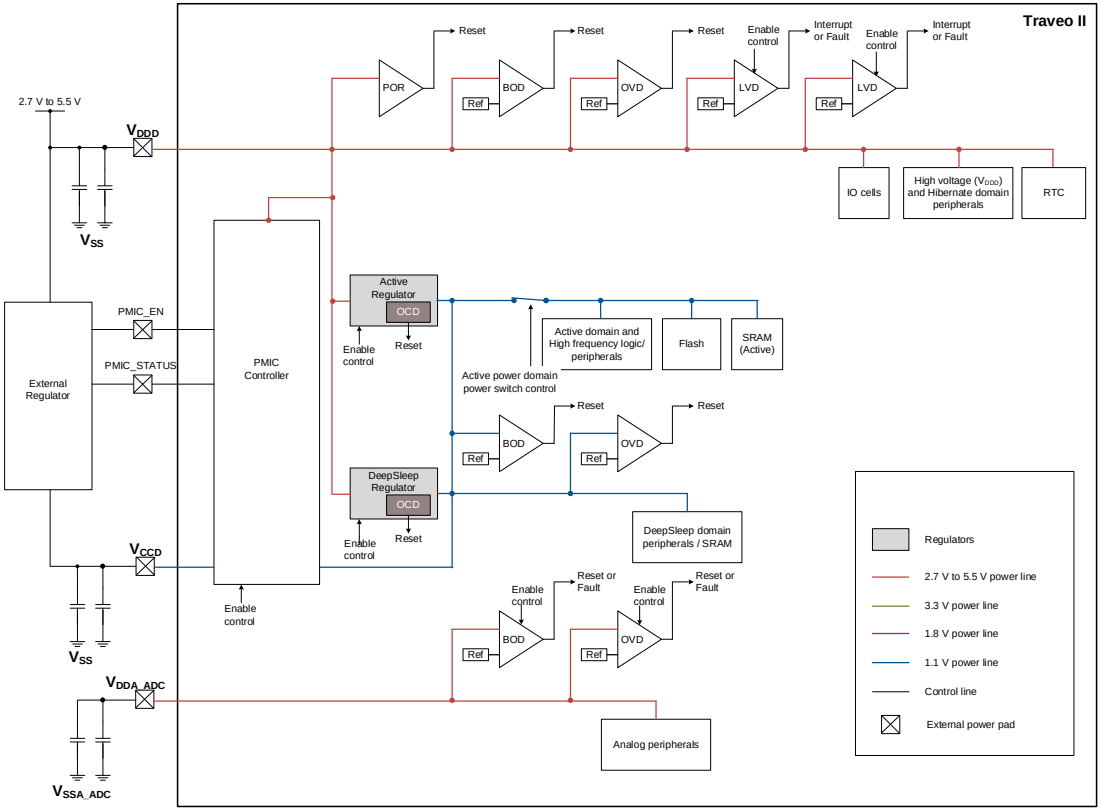
- Detects supply conditions above a threshold and applies a reset to the device
- Always on except in Hibernate and XRES modes
  - OVD on V_{DDD}
    - Generates a reset if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on V_{DDA_ADC}
    - Generates a reset, a fault, or no action (default) if a voltage excursion dips above the rising trip point
    - Supports two trip points: > 5.5 V (default) or > 5.0 V
  - OVD on V_{CCD}
    - Generates a reset if a voltage excursion dips above the rising trip point



Hint Bar

Review datasheet and TRM section 16.3.3 for additional details

Over-Current Detection (OCD) Block Diagram



Hint Bar

Review datasheet and TRM section 16.3 for additional details

OCD Features

- Detects if the device current is over the regulator limit
- Always on except in Hibernate and XRES modes
  - OCD on V_{CCD}
    - Generates a reset by detecting if the load current of a regulator is higher than expected
    - OCD is not available when using PMIC

Hint Bar

Review datasheet and TRM section 16.3.5 for additional details

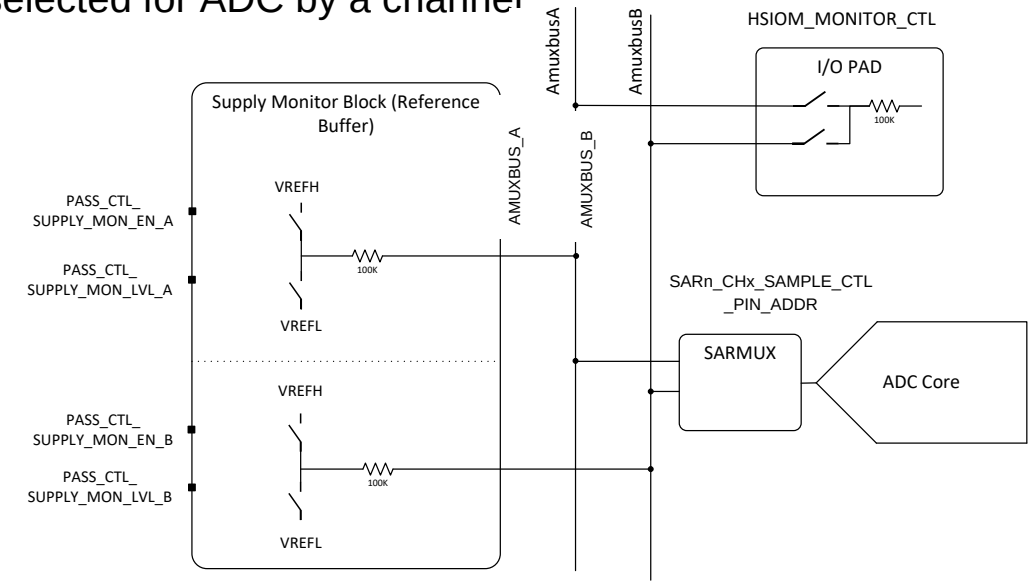
Summary of Voltage Monitoring

Monitored Supply	Monitor	Trip Point	Output	Available Power Mode
V_{DDD}	POR	1 (Fixed)	Reset	All power modes
	BOD	2 (Programmable)	Reset	All power modes except Hibernate and XRES modes
	OVD	2 (Programmable)	Reset	
	LVD	26 (Programmable)	Interrupt, Fault, or No action	
V_{DDA_ADC}	BOD	2 (Programmable)	Reset, Fault, or No action	
	OVD	2 (Programmable)	Reset, Fault, or No action	
V_{CCD}	BOD	1 (Fixed)	Reset	
	OVD	1 (Fixed)	Reset	
	OCD[1]	1 (Fixed)	Reset	

[1] Traveo II does not have the OCD for the PMIC.

Voltage Monitoring by ADC

- ADC is used for all other power supplies
- A monitor switch is provided between power/ground pad and AMUXBUS_A/B by the HSIOM_MONITOR_CTL register
- Midpoint of the signal (AMUXBUS_A/B) is connected to the SARMUX (internal signals) and can be selected for ADC by a channel
- Use case
  - V_{DDIO} monitoring



Hint Bar

Review TRM section 16.3.7 for additional details

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/Ground Pads	AMUXBUS	CYT4DN Pin No. of Package	
			BGA-500	BGA-327
Bit 0	V_{DDD}	A	G14, H20, J19, J20, K20, L20, M7, M20, N7, P7, P20, R20, T20, Y13, Y14, Y15	F10, K15, R11, M6
Bit 2				
Bit 22				
Bit 1	V_{SS}	B	A3, A24, B2, B3, B24, B25, C1, C2, C3, C8, C14, C21, C24, C25, C26, D3, D8, D14, D21, E4, F4, F25, G4, H3, H4, H25, H26, J1, J2, J3, J4, K3, K4, K10, K11, K12, K13, K14, K15, K25, K26, L4, L10, L11, L12, L13, L14, L15, L16, L17, M4, M10, M11, M12, M13, M14, M15, M16, M17, N4, N10, N11, N12, N13, N14, N15, N16, N17, P3, P4, P10, P11, P12, P13, P14, P15, P16, P17, R1, R2, R3, R4, R10, R11, R12, R13, R14, R15, R16, T4, T10, T11, T12, T13, T14, T15, T16, U4, U10, U11, U12, U13, U14, V3, V4, W3, W4, Y3, Y4, AA3, AA4, AB3, AB4, AC3, AC8, AC13, AD1, AD2, AD3, AD8, AD13, AD18, AE2, AE3, AF3, R17, T17, K17, K16	A1, A20, H13, E20, F19, G20, H9, H10, H11, H12, J8, J9, J10, J11, J12, J13, H4, K8, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L13, N1, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13, Y1
Bit 3				
Bit 6				
Bit 8				
Bit 10				
Bit 12				
Bit 21				

Hint Bar

Review TRM sections 16.3.6 and 37.10 for additional details

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/Ground Pads	AMUXBUS	CYT4DN Pin No. of Package	
			BGA-500	BGA-327
Bit 4	V_{DDIO_SMIF}	A	H8, H9, J8, K8, L8, M8	J6, G6, H6
Bit 5	$V_{DDIO\_SMIF\_HV}$	A	G7, G8, H7, J7, K7, L7	L6, K6
Bit 7	V_{DDIO_HSIO}	A	R7, T7, U7, V7, W7, Y7, Y8, Y9, Y10, Y11, Y12	N6, R7, R8, R9, R6
Bit 9	V_{DDIO_SMC}	A	G9, G10, G11, G12, G13	F7, F8, F6
Bit 11	$V_{DDIO\_GPIO\_0}$	A	G19, G20	F15
Bit 13	V_{DDA_DAC}	A	N19, N20, P19	J15
Bit 14	V_{SSA_DAC}	B	G23, G24, H24, J24, K24, L24, M24, M23	G17, G18
Bit 15	V_{DDA_ADC}	A	H17	F12
Bit 16	V_{SSA_ADC}	B	H16	D12
Bit 17	V_{REFH}	A	H18	F13
Bit 18	V_{REFL}	B	G16	D13
Bit 19	$V_{DDIO\_GPIO\_1}$	A	G17, G18, H19	F14
Bit 20	$V_{DDIO\_GPIO\_2}$	A	G15, H15	F11

Hint Bar

Review TRM sections 16.3.6 and 30.10 for additional details

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/Ground Pads	AMUXBUS	CYT3DL Pin No. of Package		
			BGA-272	TEQFP-216	TEQFP-208
Bit 0	V_{DDD}	A	M7, N7, G12, G13, F9	140	136
Bit 2					
Bit 1	V_{SSD}	B	A2, B3, C4, D4, F3, F4, K1, K2, K3, K4, R3, R4, T1, V1, R10, U10, H17, H18, F17, F18, A18, B17, A10, H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11	142 (V_{SSD})	138 (V_{SSD})
Bit 3				-	-
Bit 5				40 (V_{SSIO_HSIO})	38 (V_{SSIO_HSIO})
Bit 7				194 (V_{SSIO_SMC})	186 (V_{SSIO_SMC})
Bit 9				180 (V_{SSD})	172 (V_{SSD})
Bit 4	V_{DDIO_HSIO}	A	G4, J4, H6, J6, K6, L6, M6, N6	41	39
Bit 6	V_{DDIO_SMC}	A	F7, G6, G7	195	187
Bit 8	$V_{DDIO\_GPIO\_1}$	A	F10, F13	149	143
Bit 10	V_{SSA_DAC}	A	G15, G16	135	131
Bit 11	V_{DDA_DAC}	A	H13	132	128
Bit 12	V_{DDA_ADC}	A	F11	160	154

Hint Bar

Review TRM sections 16.3.6 and 37.10 for additional details

Power Supply Monitoring by ADC

› Relation between HSIOM_MONITOR_CTL_0 Register and Power/Ground Pins

HSIOM_MONITOR_CTL_0	Power/Ground Pads	AMUXBUS	CYT3DL Pin No. of Package		
			BGA-272	TEQFP-216	TEQFP-208
Bit 13	V_{SSA_ADC}	B	D11	161	155
Bit 14	V_{REFH}	A	F12	159	153
Bit 15	V_{REFL}	B	D12	161 (V_{SSA_ADC})	155 (V_{SSA_ADC})
Bit 16	$V_{DDIO\_GPIO\_2}$	A	F8	162	156

Hint Bar

Review TRM sections 16.3.6 and 30.10 for additional details

Appendix

Comparison between CYT2B, CYT3B/4B, and CYT3D/4D

Features		CYT2B	CYT3B/4B	CYT3D/4D
Power Supply and Monitoring	Power supply	V_{DDD} = 2.7 V to 5.5 V	V_{DDD} = 2.7 V to 5.5 V (up to 300 mA) V_{DDD} = 2.7 V to 5.5 V and V_{CCD} = 1.15 V (exceeds 300 mA)	
	5.0 V I/O power supply	V_{DDIO_1}, V_{DDIO_2}		V_{DDIO_GPIO}, V_{DDIO_SMC}
	3.3 V I/O power supply	N/A	V_{DDIO_3}, V_{DDIO_4}	V_{DDIO_HSIO}, $V_{DDIO\_SMIF\_HV}$
	1.8 V I/O power supply	N/A		V_{DDIO_SMIF}
	Analog power supply	V_{DDA}		V_{DDA_ADC}, V_{DDA_DAC}, V_{DDA_MIPI}, V_{DDA_FPD0}, V_{DDA_FPD1}, V_{DDHA_FPD0}, V_{DDHA_FPD1}, V_{DDPLL_FPD0}, V_{DDPLL_FPD1}
	Active/DeepSleep regulator	Same		
	External transistor control	N/A	Available	N/A
	External PMIC control	N/A	Available	
	POR/BOD/OVD/LVD	Same		

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Revision History

Revision	ECN	Submission Data	Description of Change
**	6629932	07/19/2019	Initial release
*A	7053309	12/16/2020	Update page 2, 4 to 11, 13 to 15, 20 to 22, 26, 27, 31. Add page 28. 29