Customer training workshop

TRAVEO™ T2G Body High and Cluster 2D CPU subsystem (CPUSS)

Q1, 2024

public

Target products

› Target product list for this training material:

Family category	Series	Code flash memory size
TRAVEO™ T2G Automotive Body Controller High	CYT3BB/4BB	Up to 4160 KB
TRAVEO™ T2G Automotive Body Controller High	CYT4BF	Up to 8384 KB
TRAVEO™ T2G Automotive Body Controller High	CYT6BJ	Up to 16768 KB
TRAVEO™ T2G Automotive Cluster	CYT3DL	Up to 4160 KB
TRAVEO™ T2G Automotive Cluster	CYT4DN	Up to 6336 KB

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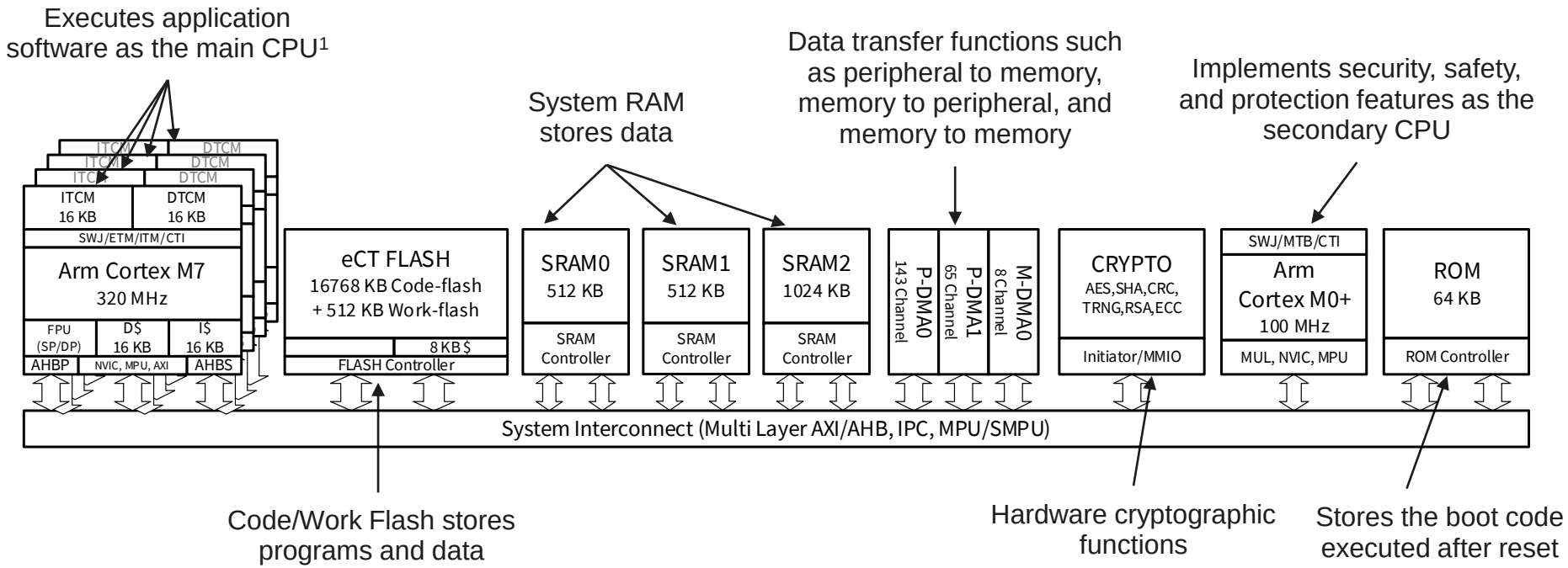
CPU subsystem overview

› The CPU subsystem (CPUSS) is based on dual 32-bit Arm® Cortex® CPUs.

CPU subsystem components



Hint Bar

Review TRM section 4.1 for additional details specific to the CPUSS

[1] CYT6 series have four Cortex-M7 CPUs, CYT4 series have two Cortex-M7 CPUs, and CYT3 series have single Cortex-M7 CPU

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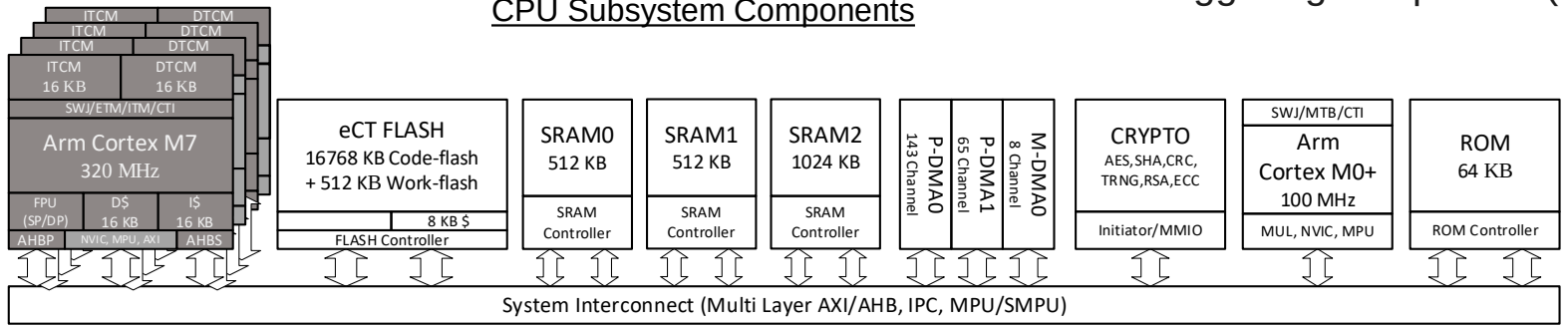
Cortex®-M7 features summary

- Main CPU
  - Up to four Cortex®-M7 CPUs[1]
  - Execution of application software
  - Up to 350-MHz operation (CYT4BF)[2]
  - Up to 320-MHz operation (CYT4DN,CYT6BJ[2]
- Tightly-coupled memories (ITCM and DTCM) and instruction and data caches[3]
- System tick (SysTick) timer
- Floating-point unit (FPU)
  - Single and double precision
  - Compliant with the ANSI/IEEE Std 754-2008 IEEE Standard for Binary Floating-Point Arithmetic
- Memory protection unit (MPU)
  - Sixteen protection regions
  - Privileged/unprivileged, read/write attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, eight interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supported SWD and JTAG interface (SWJ)
  - Tracing components (ETM/ITM over ETB/TPIU)
  - Cross-triggering component (CTI)

CPU Subsystem Components



[1] CYT6 series have four Cortex-M7 CPUs, CYT4 series have two Cortex®-M7 CPUs, and CYT3 series have single Cortex®-M7 CPU
[2] See the device datasheet for operation frequency of target product.
[3] See the device data sheet for supported capacity of ITCM, DTCM and caches.

Hint Bar

Arm® provides additional reference material on their webpage at: infocenter.arm.com

Training section references:

- Interrupts

- Program and debug interface

- Protection units

- SRAM interface

Combined SWD/JTAG interface (SWJ)

Embedded trace macrocell (ETM)

Instrumentation trace macrocell (ITM)

Cross-triggering interface (CTI)

Embedded trace buffer (ETB)

Trace port interface Unit (TPIU)

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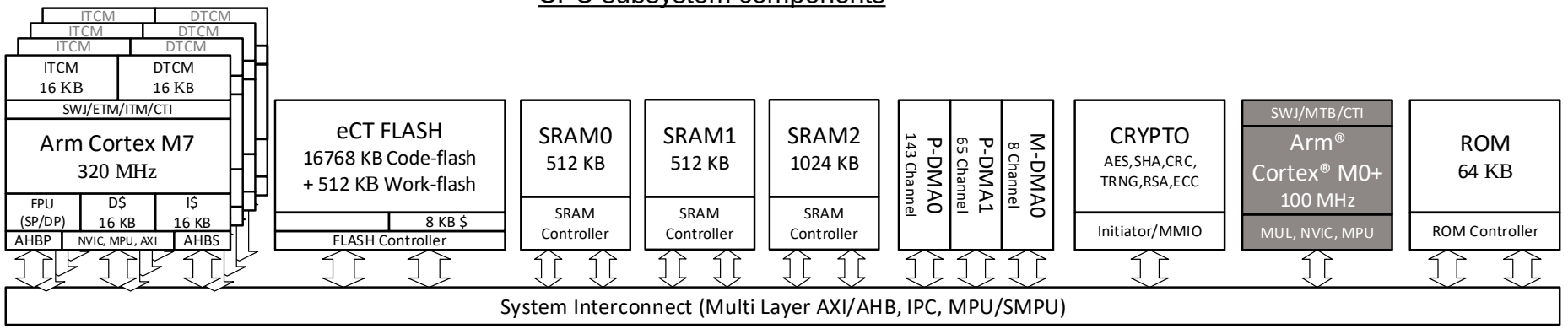
Cortex®-M0+ features summary

- Secondary CPU
  - Execution of boot process
  - Secure master in secure system to establish a root-of-trust
  - Up to 100-MHz operation[1]
- SysTick timer
- Memory protection unit (MPU)
  - Eight protection regions
  - Privileged/unprivileged access attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, four interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supported SWD and JTAG interface (SWJ)
  - Tracing component (ETM over MTB)
  - Cross-triggering component (CTI)

CPU subsystem components



Hint Bar

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Training section references:

- Interrupts

- Program and debug interface

- Protection units

Combined SWD/JTAG interface (SWJ)

Micro trace buffer (MTB)

Embedded trace macrocell (ETM)

Cross-triggering interface (CTI)

[1] For CM4 to operate at 160 MHz, CM0+ is required to operate at a frequency of 80 MHz. See the device datasheet for operation frequency of target product.

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CPUSS dedicated master identifier

- Each bus master has a dedicated master identifier, which is used for:
  - Bus arbitration
  - IPC lock acquire functionality
  - Violation access information by MPU, SMPU, and PPU

Master Identifier[1]	Bus Master (CYT6BJ)	Bus Master (CYT4DN)
0	Cortex®-M0+	Cortex®-M0+
1	Crypto	Crypto
2	P-DMA 0	P-DMA 0
3	P-DMA 1	P-DMA 1
4	M-DMA	M-DMA
5	SDHC	-
7	Cortex-M7_2	-
8	Cortex-M7_3	-
9	Ethernet 0	Ethernet 0
10	Ethernet 1	JPEG Decorder
11	-	AXI DMA
12	-	Video Subsystem
13	Cortex-M7_1	Cortex-M7_1
14	Cortex-M7_0	Cortex-M7_0
15	DAP Tap Controller	DAP Tap Controller

Hint Bar

Inter processor communication (IPC)

Memory protection unit (MPU)

Shared memory protection unit (SMPU)

Peripheral protection unit (PPU)

[1] See the device datasheet for master identifier number and regarding peripherals of target product.

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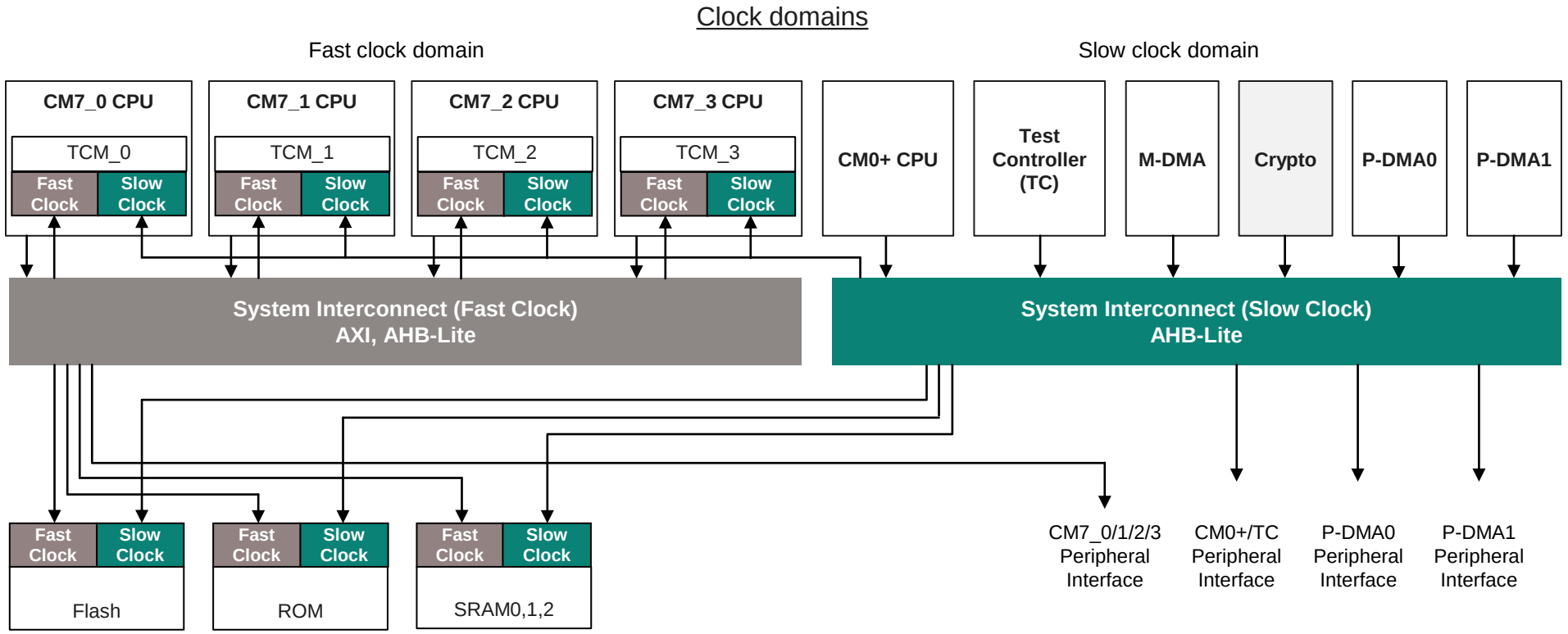
CPUSS bus infrastructure

- AHB-Lite and AXI bus infrastructure
- Bus clock domains
  - Fast/slow clock domains
  - Each memory interface has both domains
- Bus competition
  - CPUSS has multiple bus masters
  - Design a system that considers bus competition by simultaneous access



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Sys Interface in CM7 can only access peripherals

Code Interface in CM7 can only access memory controllers

Training section references:

- Clock System

- SRAM interface

- Flash

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CPU features

- **Cortex®-M7**
  - 5 CoreMark/MHz and 2.14 DMIPS/MHz
  - ISA Support (Thumb/Thumb-2)
  - 6-stage superscalar + branch prediction pipeline
  - Interconnect
    - AXI master
    - AHB peripheral port (AHBP/AHBS)
    - Tightly-coupled memory (ITCM/DTCM)
  - Instruction and data cache
  - DSP extensions
    - Single-cycle 16/32-bit MAC, single-cycle dual 16-bit MAC
    - 8/16-bit SIMD arithmetic
  - Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - Nested vector interrupt controller (NVIC)
    - Vector table relocation (VTOR)
  - Wake-up Interrupt Controller(WIC)
  - SysTick Timer

- **Cortex®-M0+**
  - 1.99 CoreMark/MHz and 0.9 DMIPS/MHz
  - ISA Support (Thumb/Thumb-2)
  - 2-stage Pipeline
  - Interconnect
    - AHB - Lite
  - Memory Protection Unit (MPU)
  - Nested vector interrupt controller (NVIC)
    - Vector table relocation (VTOR)
  - Wake-up Interrupt Controller(WIC)
  - SysTick Timer

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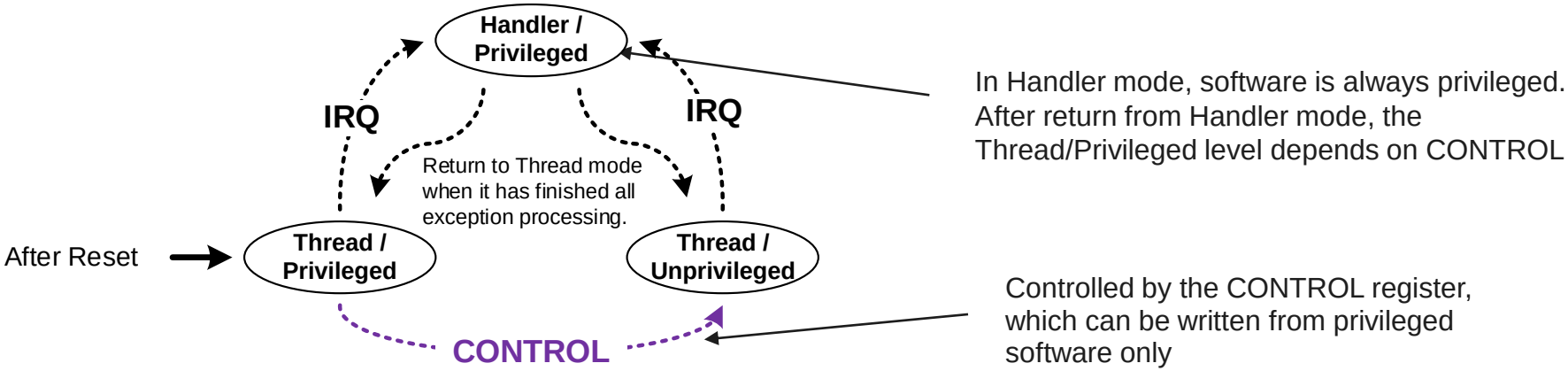
CPU mode transition

- Both CPUs support two operating modes and two privilege levels:
  - Operating mode
    - Thread mode executes application software
    - Handler mode handles exceptions
  - Privilege levels
    - Unprivileged: Software has limited access to MSR/MRS instructions (uses CPS instructions), system timer, NVIC, system control block, and memory/peripherals
    - Privileged: Software can use all instructions and has access to all resources

Transition from Thread/Privileged to Thread/Unprivileged by CONTROL register[1]
Transition from Thread/Unprivileged to Thread/Privileged via SVC[2]



In Handler mode, software is always privileged. After return from Handler mode, the Thread/Privileged level depends on CONTROL

Controlled by the CONTROL register, which can be written from privileged software only

Hint Bar

Review TRM section 4.5 for additional details specific to CPU modes

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Move to system coprocessor register from the Arm register (MSR)

Move the contents of program status register to a general-purpose register (MRS)

Change processor state (CPS)

[1] The CONTROL register is a CPU-specific register. It defines privileged/unprivileged, stack pointer, and FPU extension.
[2] Supervisor calls are used to request privileged operations

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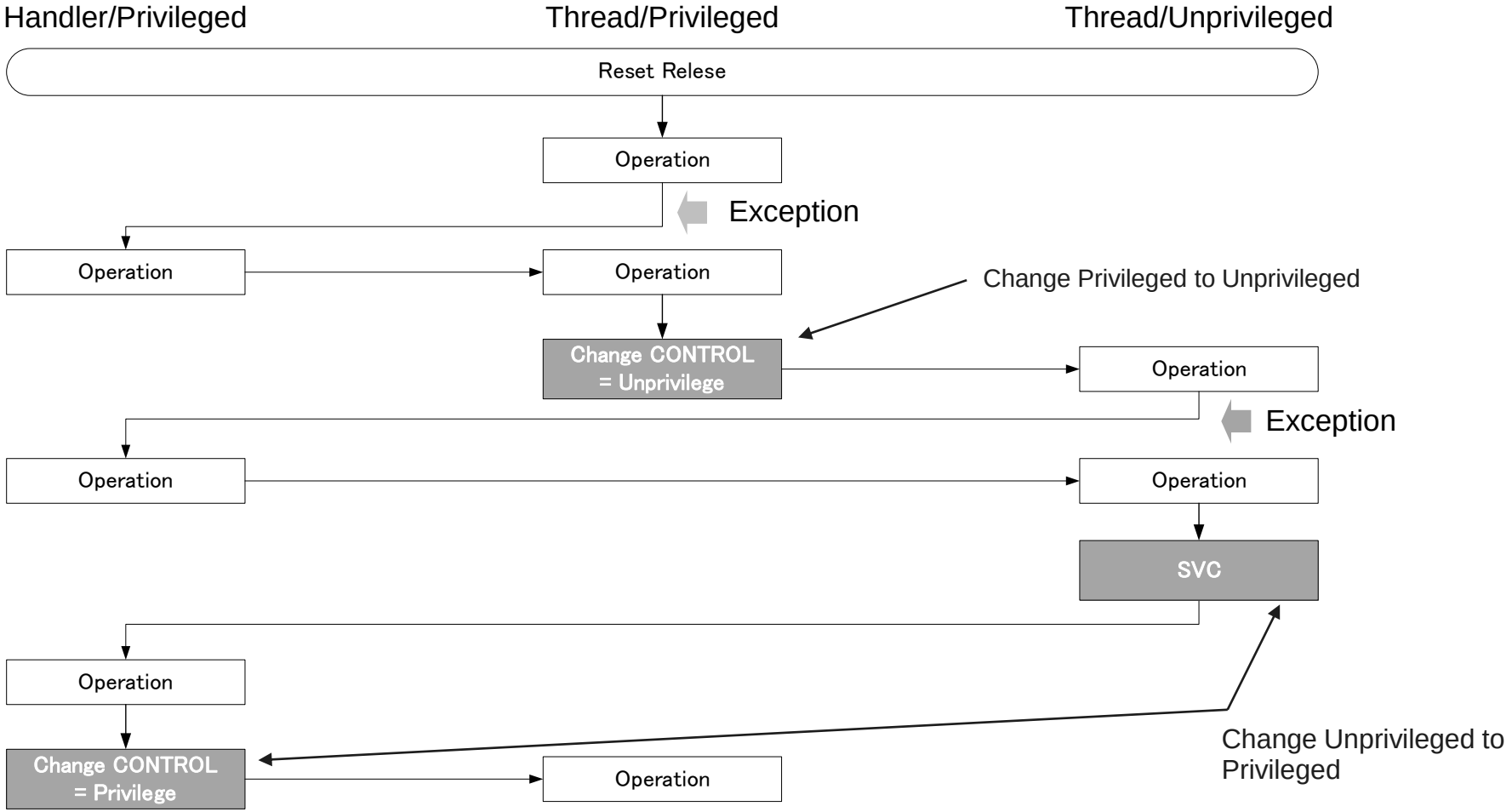
Operation modes transition

› Use Case: Changing Privileged/Unprivileged mode



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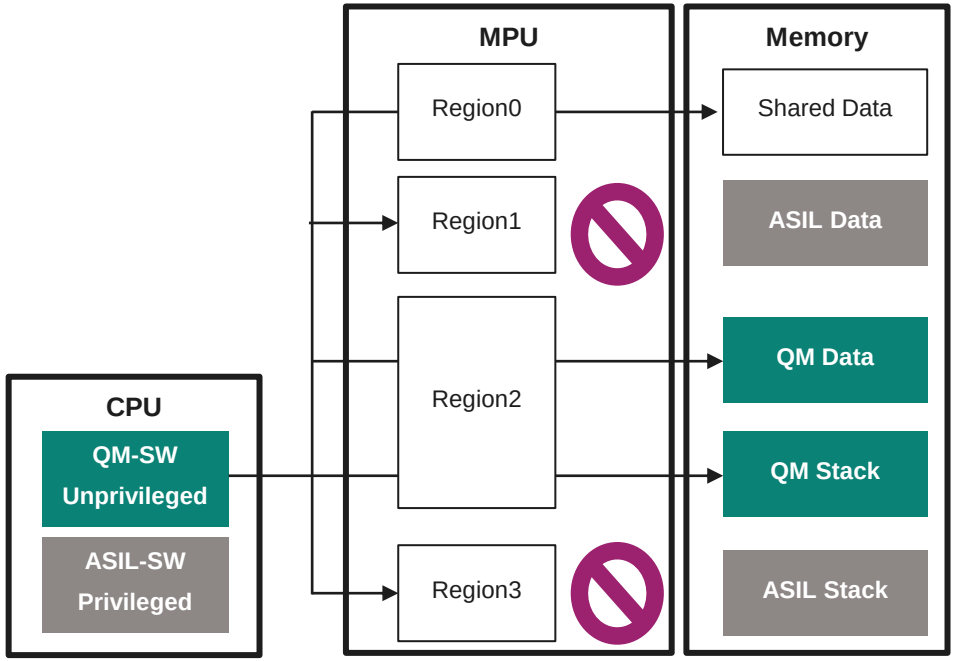
Memory Protection

- Each CPU has a memory protection unit (MPU)[1] that:
  - Realizes software separation freedom of interface
  - Includes address range, read/write, and privileged/unprivileged attributes
  - Features sixteen protection regions
- Use case
  - Software partitioning of ASIL and QM in Functional Safety

Example of MPU Operation



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[1] MPU registers are written by privileged software and are only one part of the protection concept. For details, refer to the Protection Units training section.

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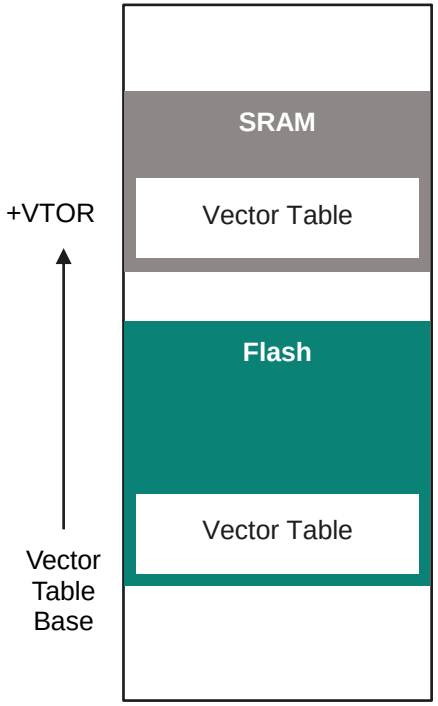
Vector table relocation

- **Vector Table Offset Register (VTOR)[1]**
  - Defines the location of the vector table of each core. There is a VTOR for each CM7 and another one for CM0.
  - Can be used to relocate the vector table from Flash to SRAM, allowing the interrupt handlers to change dynamically
  - VTOR is written from privileged software only
  - Use the following registers to set VTOR for both cores:
    - CM0_VECTOR_TABLE_BASE: By default, set to beginning of Flash by Boot ROM
    - CM7_x_VECTOR_TABLE_BASE: Set by CM0+ application before releasing the CPU core CM7_x from reset [2]
  - After boot, each core copies the vector table to SRAM and updates VTOR with the address of the new location
- **Use cases**
  - Execute the program with RAM only, for Flash programming or performance improvement
  - Use different vectors depending on software level or system mode, such as normal and reprogramming

VTOR Operation



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See the Register TRM for additional details

[1] The VTOR register is a CPU-specific register
[2] The 'x' denotes the CM7 core number

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System Tick generation

- Each CPU supports a SysTick timer to measure time duration, which provides:
  - A 24-bit down counter
  - A selectable internal CPU clock or external clock
  - Active and Sleep mode operation
  - SysTick interrupt generation
- SysTick registers can be written from Privileged software only

- Use Cases
  - RTOS tick timer
  - Alarm timer to alert when an action is not completed within a particular duration
  - Software completion time measurement

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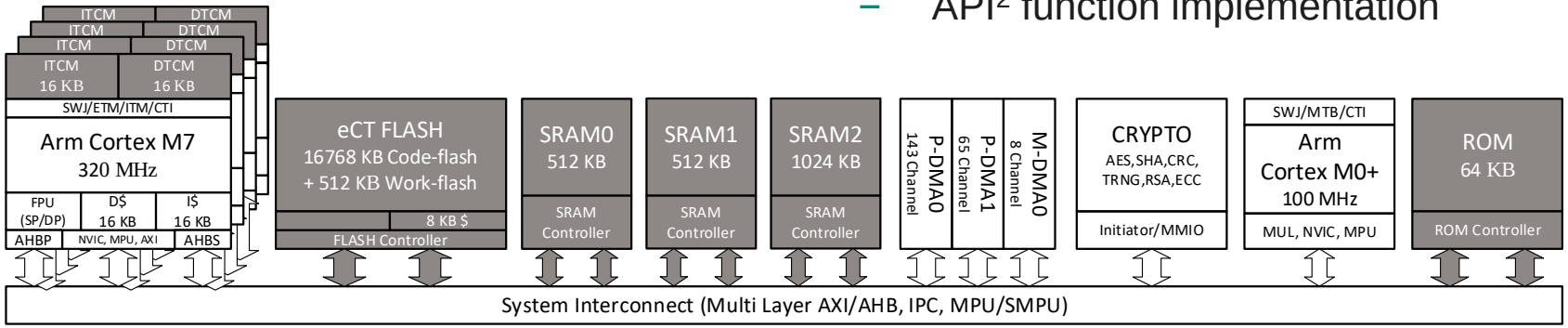
CPU subsystem memory feature summary

- TCM
  - ITCM and DTCM (instruction/data tightly coupled memory) for CM7
  - Size 16KB: ITCM/16KB: DTCM (CYT4BF, CYT6BJ)[1]
    64KB: ITCM/64KB: DTCM(CYT4DN) [1]
  - Error-correction code (ECC) function (SEC/DED)
- SRAM
  - Data storage and code execution
  - Size: up to 1024KB(CYT4BF) [1]
    up to 2048KB(CYT6BJ) [1]
    up to 640KB(CYT4DN) [1]
  - Each CPU sharing
  - ECC function
- Flash
  - Code and Work Flash
  - Size: up to 8MB: Code/ 256KB: Work (CYT4BF) [1]
    up to 8MB x 2: Code/ 256KB x 2: Work (CYT6BJ) [1]
    up to 6MB: Code/ 128KB: Work (CYT4DN) [1]
  - ECC function
  - Instruction cache for each CPU
  - APIs for Flash programming
- ROM
  - Boot code for CM0+
  - API[2] function implementation



Hint Bar

Training section references:

- Flash

- SRAM interface

- Boot

[1] See the device datasheet for memory size of target product.
[2] No user access to read or modify SROM code

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P-DMA/M-DMA feature summary

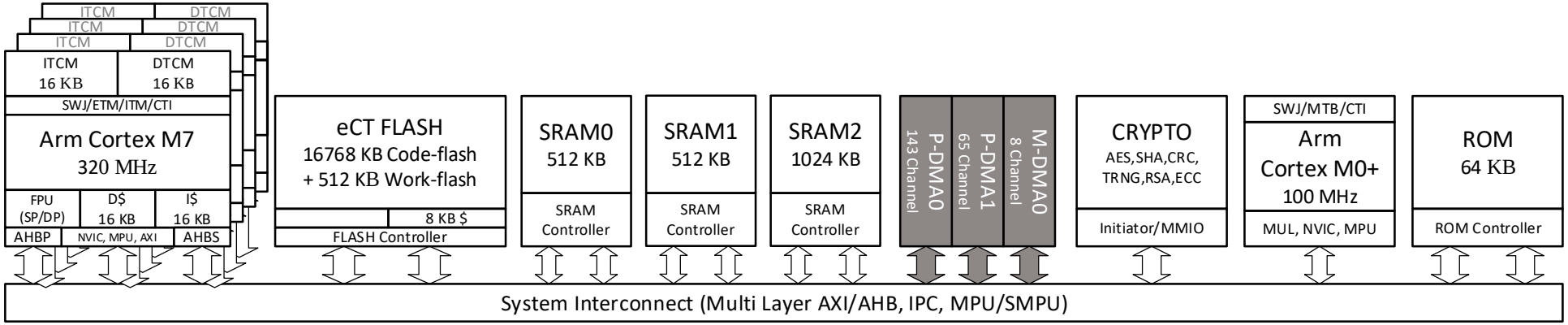
- Peripheral DMA (P-DMA)
  - Single transfer engine shared for all channels
  - Focuses on low-latency transfer
  - Transfer modes:
    - Single, 1D, 2D, and CRC
- Memory DMA (M-DMA)
  - Dedicated transfer engine for each channel
  - Focuses on high-memory bandwidth
  - Transfer modes:
    - Single, 1D, 2D, Memory Copy, and Scatter

Hint Bar

Training section references:

- Direct Memory Access

CPU Subsystem Components



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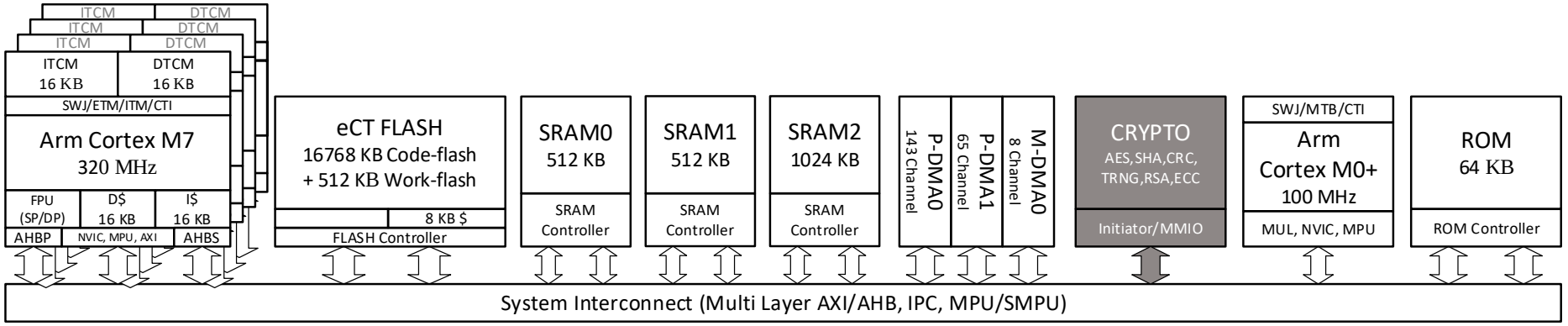
Cryptographic (Crypto) feature summary

- Hardware Crypto functions[1]
  - Symmetric key encryption and decryption
  - Hashing
  - Message authentication
  - Random number generation
  - Cyclic redundancy checking
  - Asymmetric key cryptography

CPU Subsystem Components



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Training section references:

- Device Security

[1] Access limited to the secure master (CM0+)

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Appendix

Comparison between families

Features		Body Controller Entry (CYT2BL)	Body Controller High (CYT6BJ)	Body Controller High (CYT4BF)	Cluster (CYT4DN)
Main CPU	CPU	Cortex-M4 CPU	Four Cortex-M7 CPUs	Two Cortex-M7 CPUs	
	Operating Frequency	Up to 160 MHz	Up to 320 MHz	Up to 350 MHz	Up to 320 MHz
	FPU	Single-precision	Single/double-precision		
	Cache	N/A	16KB instruction, 16KB data		
	MPU	Cortex-M4: 8 regions	Cortex-M7: 16 regions		
	Interrupt Structure	NVIC+WIC			
	System Tick Timer	Supported			
Secondary CPU	CPU	Cortex-M0+ CPU			
	Operating Frequency	Same (Up to 100 MHz)			
	MPU	Cortex-M0+: 8 regions			
	Interrupt Structure	NVIC+WIC			
	System Tick Timer	Supported			
Flash	Bus Interface	AHB-Lite	AXI, AHB-Lite		
	ECC (SEC/DED)	Supported			
	Bank Modes	Supported			
	Size (Code/Work)	4MB / 128KB	16MB / 512KB	8MB / 256KB	6MB / 128KB
SRAM	Bus Interface	AHB-Lite	AXI, AHB-Lite		
	ECC (SEC/DED)	Support			
	TCM Size	N/A	16KB ITCM, 16KB DTCM		64KB ITCM,64KB DTCM
	SRAM Size	512KB	2048KB	1024KB	640KB
Boot		Supported			
Device Security with Crypto		Supported			
Direct Memory Access	P-DMA	Supported			
	M-DMA	Supported			

[1] This functionality is for debug purposes

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6381034	11/12/2018	Initial release
*A	6633371	7/22/2019	Updated page 2, 3 to 6, 14 to 16, 18. Added page 8.
*B	7060645	01/06/2021	Updated Slide 2, 4, 6, 14
*C	8013047	03/15/2024	Updated Slide 2, 3 to 7, 14 to 16, 18.

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